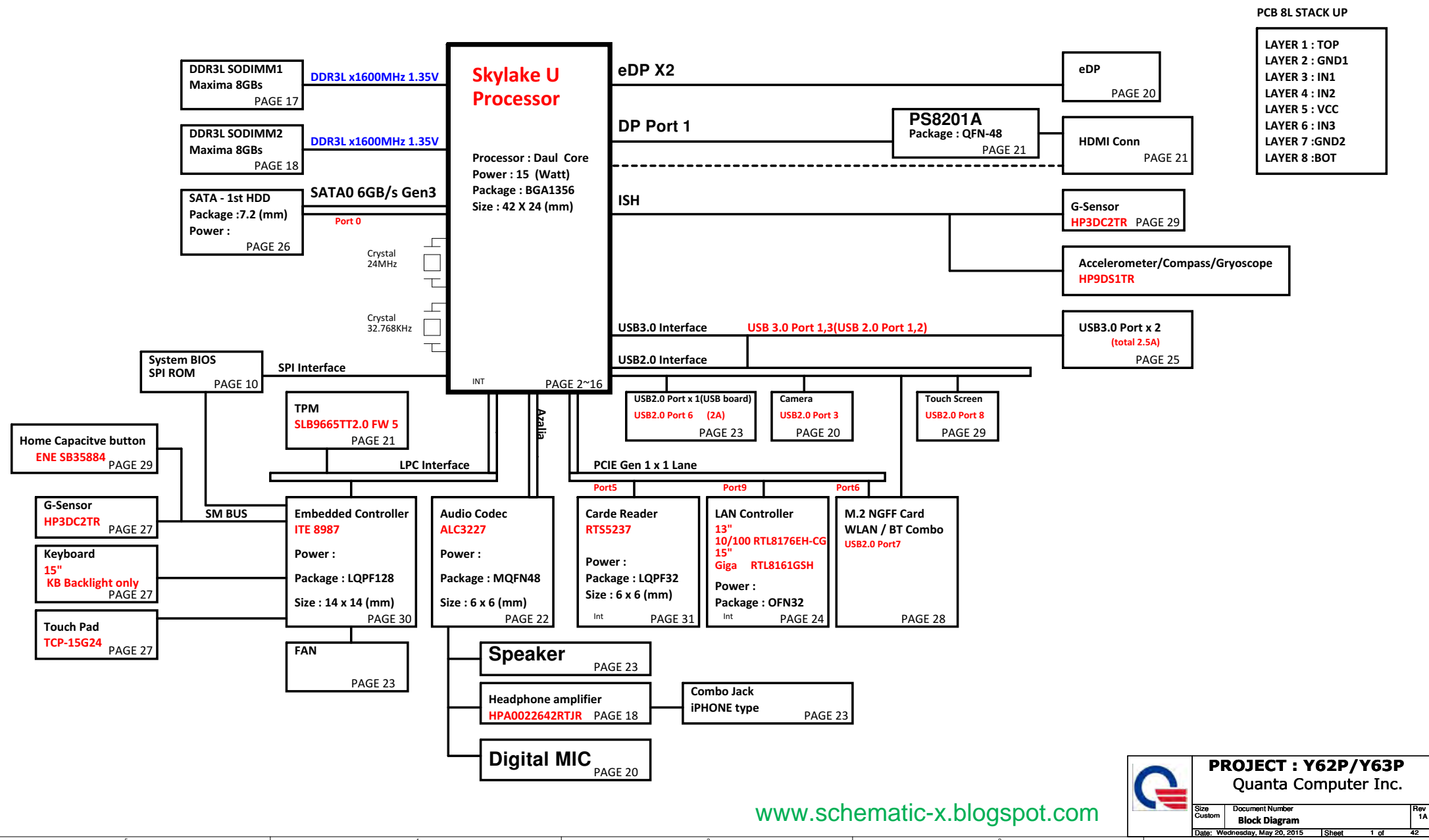
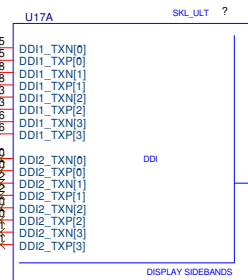
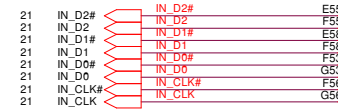


# 13"/15" Intel Skylake ULT Platform Block Diagram

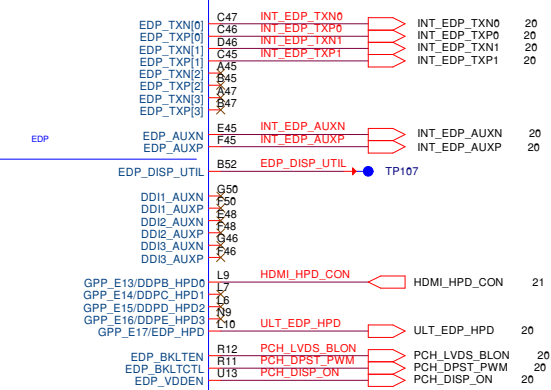




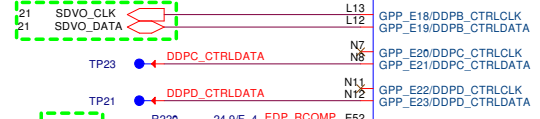
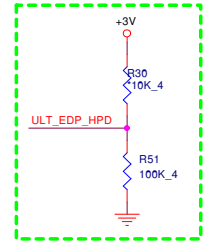
HDMI



Need apply PN



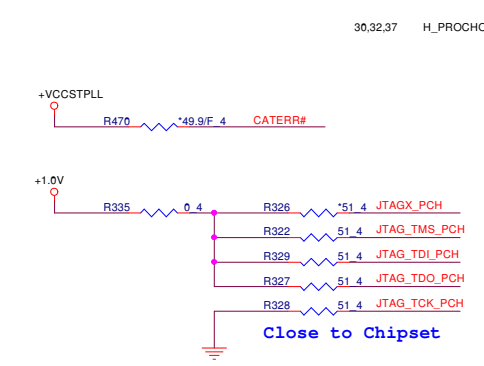
Reserve EDP\_HPD opposites circuit!



eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

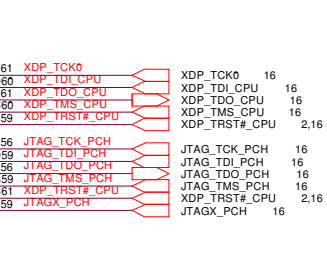
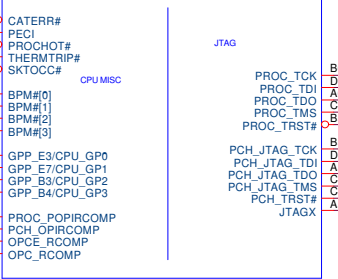
SKL\_ULT  
REV = 1

1 OF 20

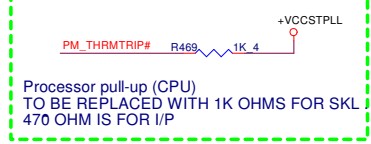


Close to Chipset

Need apply PN

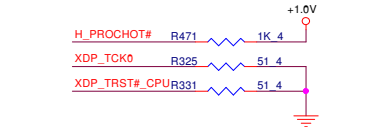
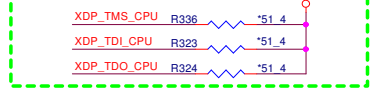


Close to EC

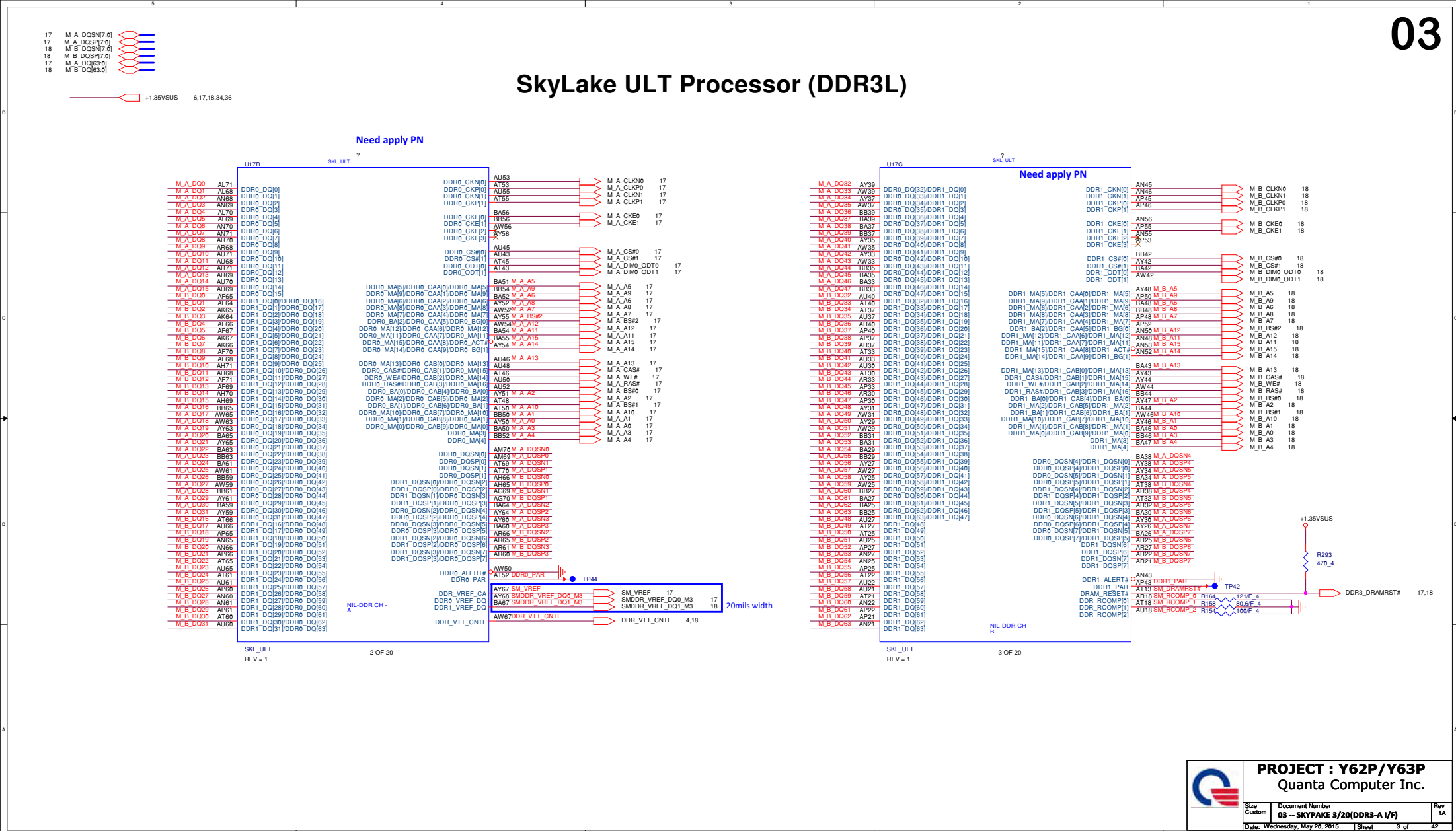


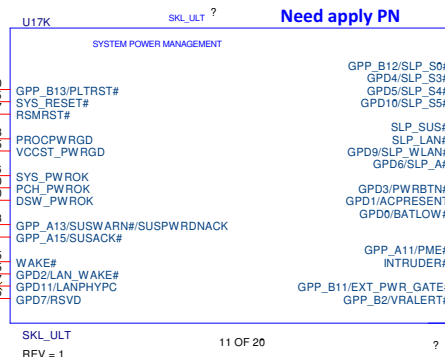
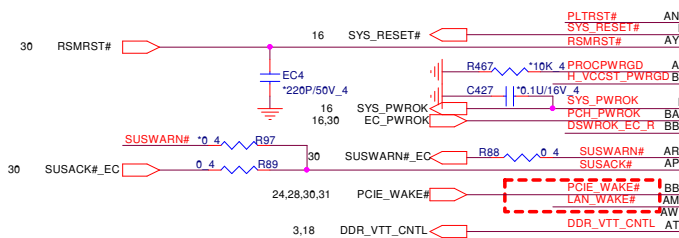
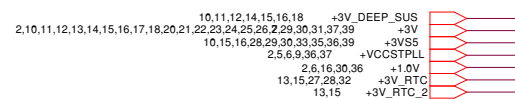
Processor pull-up (CPU)  
TO BE REPLACED WITH 1K OHMS FOR SKL  
470 OHM IS FOR I/P

PLACE NEAR CPU

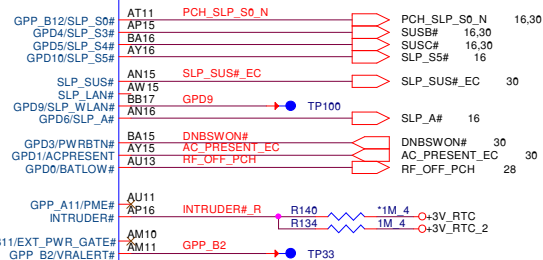


## SkyLake ULT Processor (DDR3L)

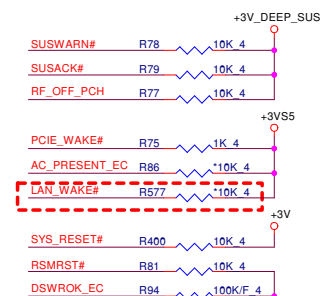




Need apply PN

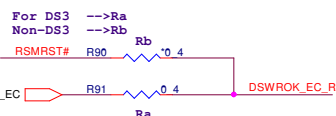


## PCH Pull-high/low(CLG)



0508 LAN\_WAKE# reserve 10K OHM to +3VS5

## For DS3 Sequence

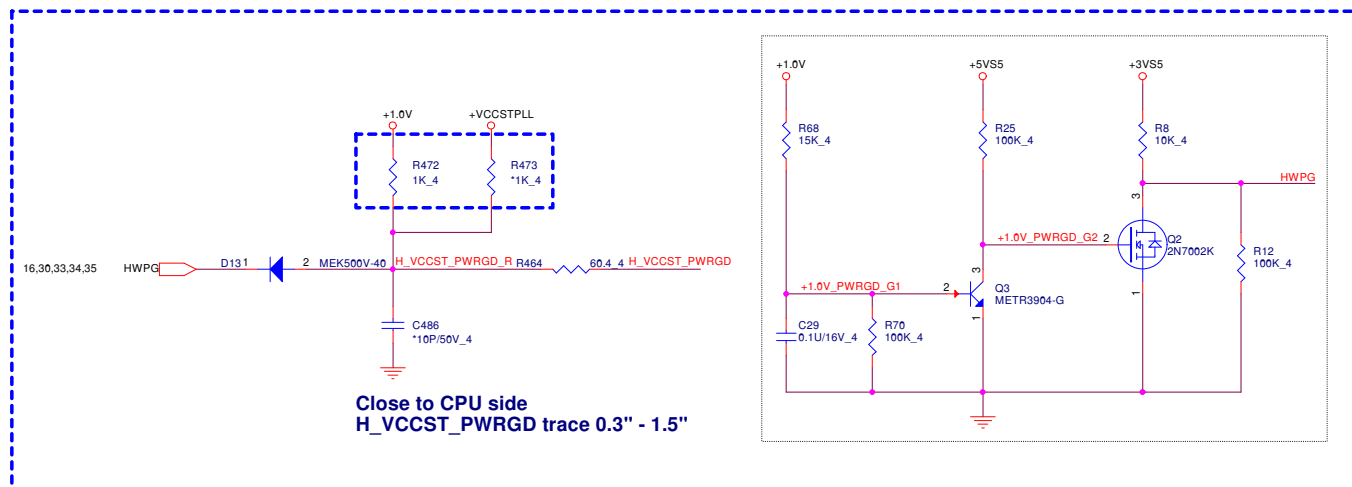
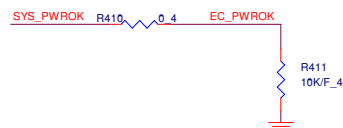


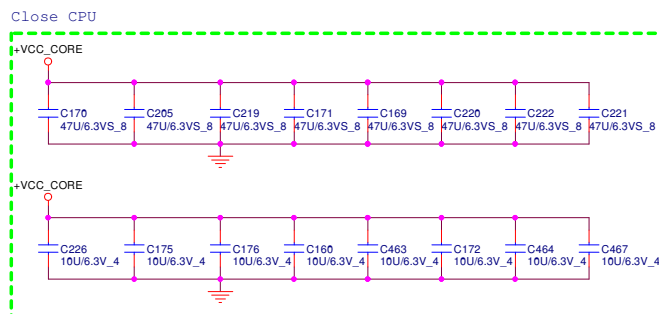
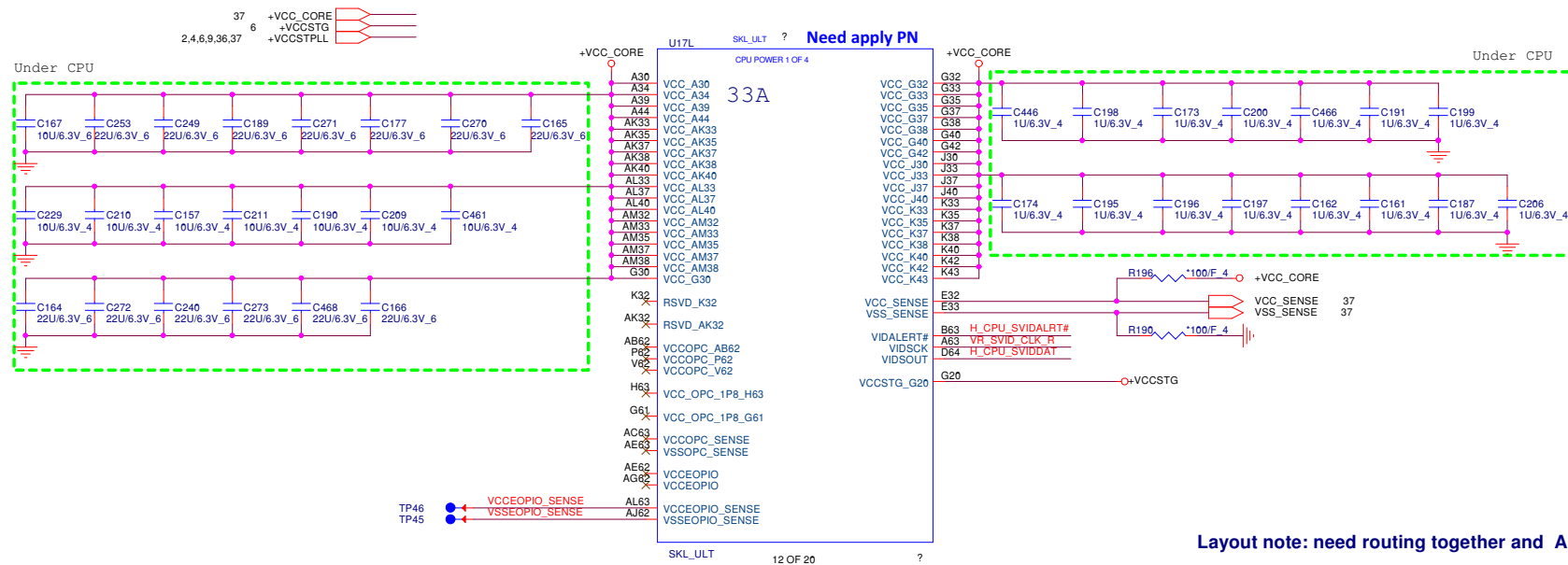
## PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns



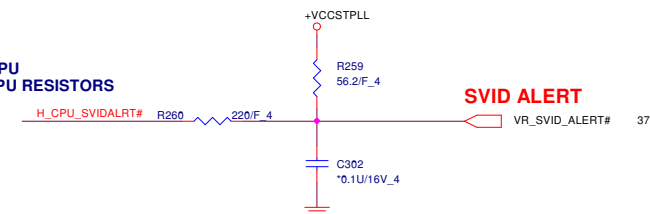
## System PWR\_OK(CLG)

Close to CPU side  
H\_VCCST\_PWRGD trace 0.3" - 1.5"

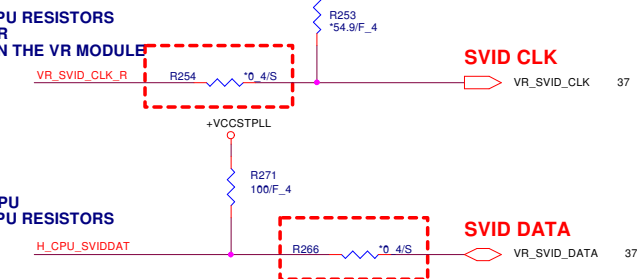


Layout note: need routing together and ALERT needbetween CLK and DATA.

CLOSE TO CPU  
PLACE THE PU RESISTORS



PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE



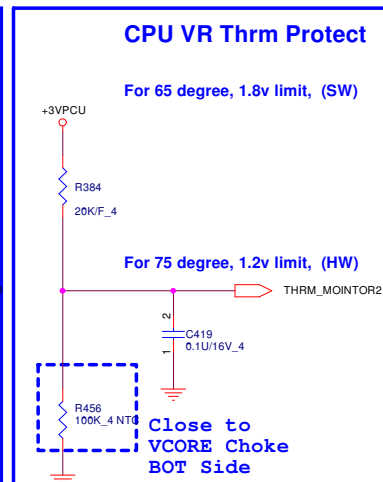
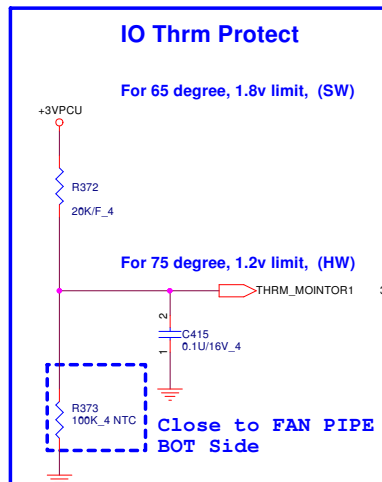
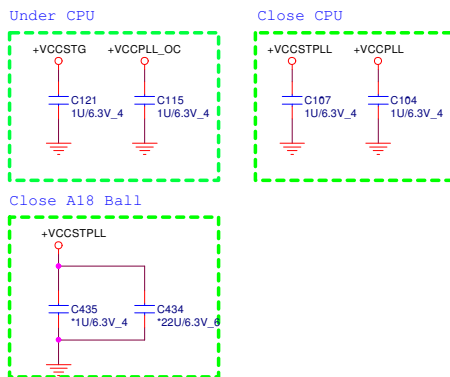
0506 Change R254, R266 from 0 OHM to shurtpad

| Power Rail             | Description   | Control                                |
|------------------------|---|--|
| V <sub>CC</sub>        | Processor IA Cores Power Rail   | SVID                                   |
| V <sub>CCGT</sub>      | Processor Graphics Power Rails  | SVID                                   |
| V <sub>CCGTx</sub>     | Processor Graphics Extended Power Rail<br>Available only for GT3/GT4 processor SKUs | SVID                                   |
| V <sub>CCSA</sub>      | System Agent Power Rail   | SVID/Fixed<br>(SKU dependent)          |
| V <sub>CCIO</sub>      | IO Power Rail   | Fixed                                  |
| V <sub>CCST</sub>      | Sustain Power Rail  | Fixed                                  |
| V <sub>CCPLL</sub>     | Processor PLLs power rail   | Fixed                                  |
| V <sub>DDQ</sub>       | Integrated Memory Controller Power Rail   | Fixed (Memory<br>technology dependent) |
| V <sub>CCOPC</sub>     | Processor OPC power rail (available only in SKU's with OPC)                         | Fixed                                  |
| V <sub>CCOPC_1P8</sub> | Processor OPC power rail (available only in SKU's with OPC)                         | Fixed                                  |
| V <sub>CCEOPIO</sub>   | Processor EOPIO power rail (available only in SKU's with OPC)                       | Fixed                                  |

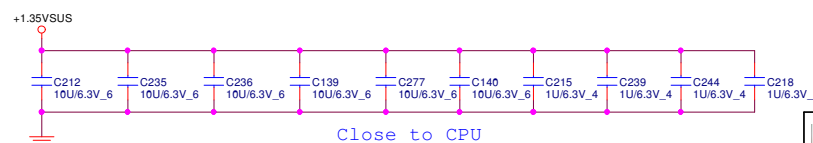


**PROJECT : Y62P/Y63P**  
**Quanta Computer Inc.**

|                               |   |           |
|-------------------------------|---|-----------|
| Size<br>Custom                | Document Number<br><b>05 - SKYPAKE 6/20 (POWER-1)</b> | Rev<br>1A |
| Date: Wednesday, May 20, 2015 | Sheet   | 5 of 42   |



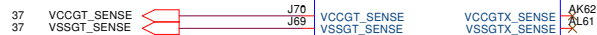
| Power Rail             | Description   | Control                             |
|------------------------|---|-------------------------------------|
| V <sub>CC</sub>        | Processor IA Cores Power Rail   | SVID                                |
| V <sub>CCGT</sub>      | Processor Graphics Power Rails  | SVID                                |
| V <sub>CCGTX</sub>     | Processor Graphics Extended Power Rail<br>Available only for GT3/GT4 processor SKUs | SVID                                |
| V <sub>CCSA</sub>      | System Agent Power Rail   | SVID/Fixed (SKU dependent)          |
| V <sub>CCIO</sub>      | IO Power Rail   | Fixed                               |
| V <sub>CCST</sub>      | Sustain Power Rail  | Fixed                               |
| V <sub>CCPLL</sub>     | Processor PLLs power rail   | Fixed                               |
| V <sub>DDQ</sub>       | Integrated Memory Controller Power Rail   | Fixed (Memory technology dependent) |
| V <sub>CCOPC</sub>     | Processor OPC power rail (available only in SKU's with OPC)                         | Fixed                               |
| V <sub>CCOPC_1P8</sub> | Processor OPC power rail (available only in SKU's with OPC)                         | Fixed                               |
| V <sub>CCEOPIO</sub>   | Processor EOPIO power rail (available only in SKU's with OPC)                       | Fixed                               |



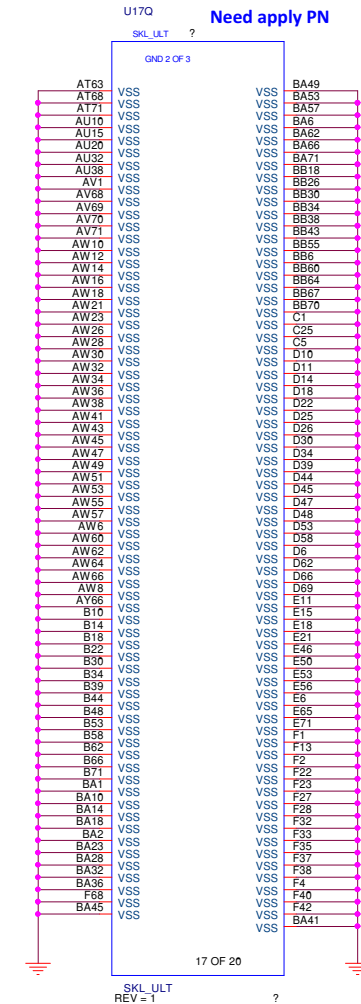
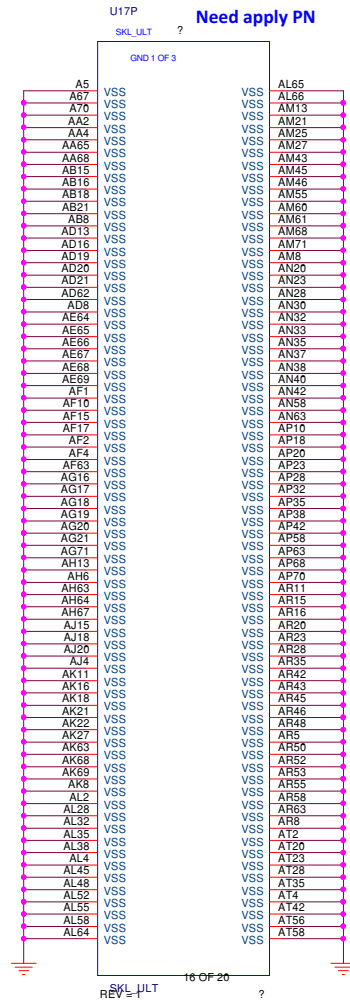
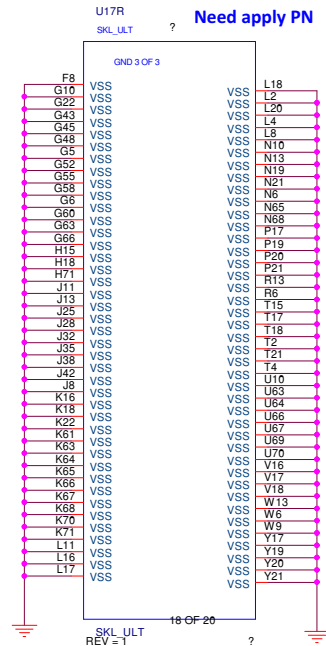
**PROJECT : Y62P/Y63P**  
Quanta Computer Inc.

|                               |  |           |
|-------------------------------|--|-----------|
| Size<br>Custom                | Document Number<br><b>06 -- SKYPAKE 7/20 (POWER-2)</b> | Rev<br>1A |
| Date: Wednesday, May 20, 2015 | Sheet  | 6 of 42   |

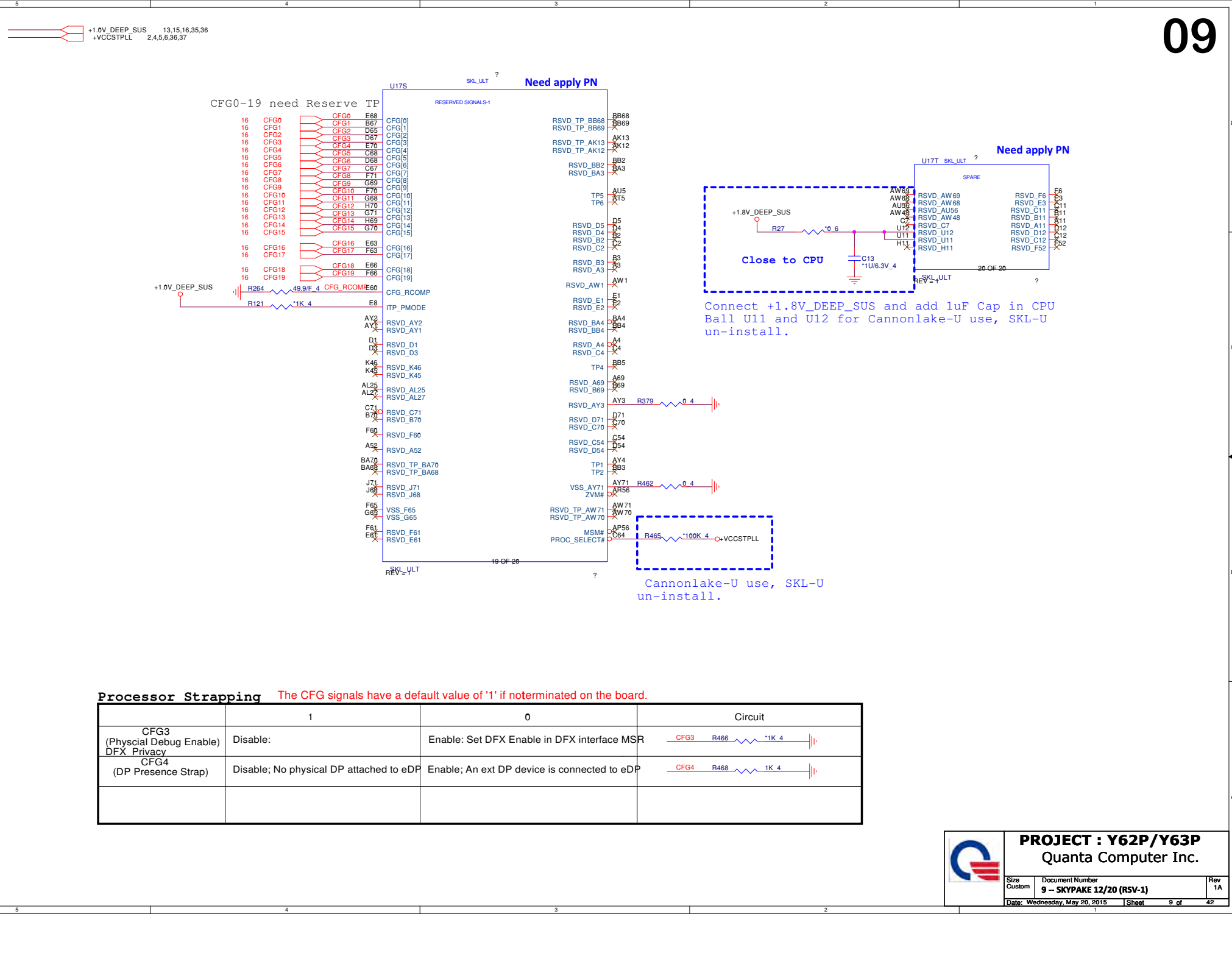




SKL\_ULT 13 OF 20  
REV = 1





[illegible]

09

**CFG0-19 need Reserve TP**

**Need apply PN**

**Need apply PN**

**Close to CPU**

**Cannonlake-U use, SKL-U un-install.**

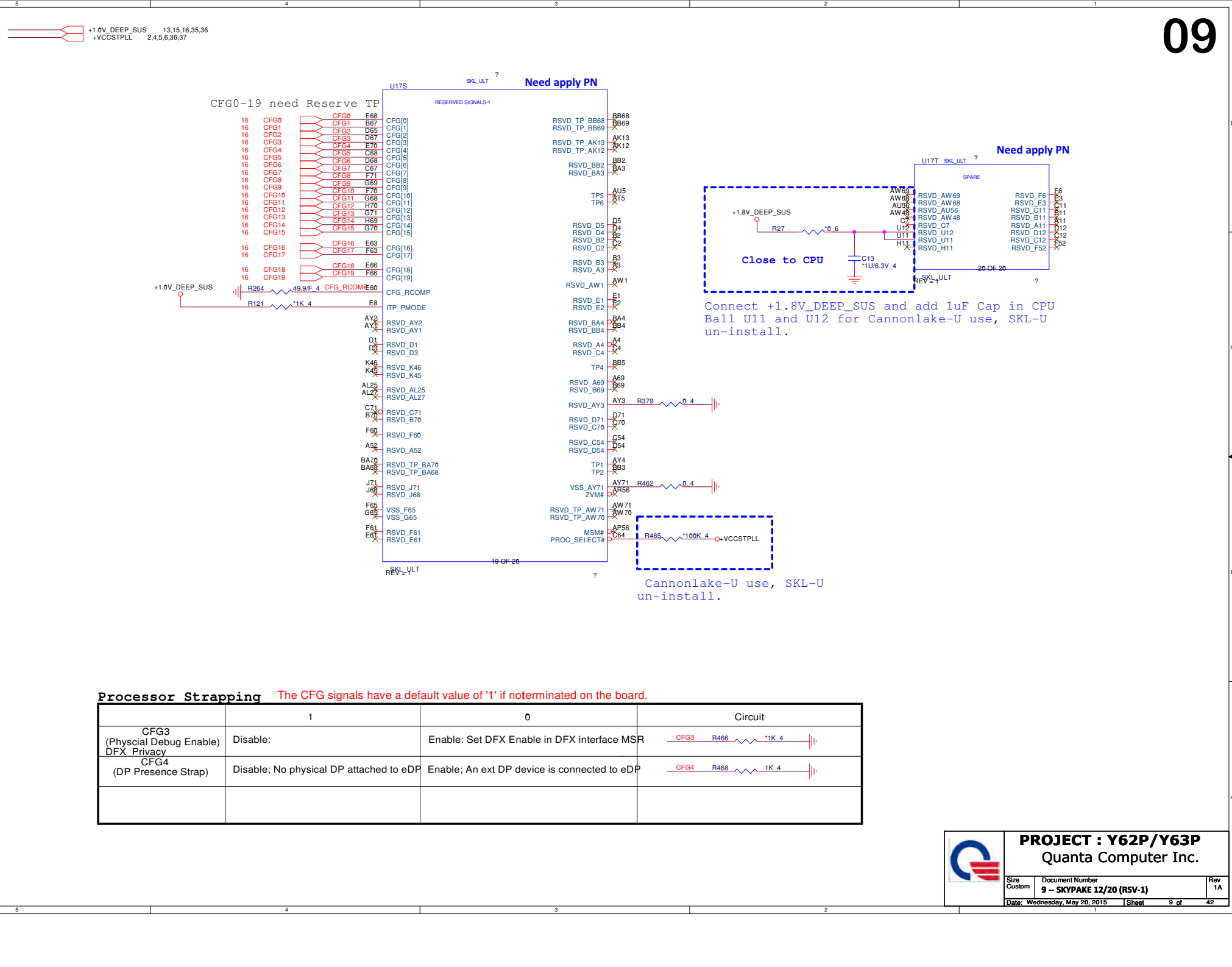
### Processor Strapping

The CFG signals have a default value of '1' if notterminated on the board.

|  | 1                                       | 0  | Circuit        |
|--|---|--|----------------|
| CFG3<br>(Physical Debug Enable)<br>DFX_Privacy | Disable:                                | Enable: Set DFX Enable in DFX interface MSR  | CFG3 R466 1K 4 |
| CFG4<br>(DP Presence Strap)                    | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP | CFG4 R468 1K 4 |
|  |   |  |                |

**PROJECT : Y62P/Y63P**  
**Quanta Computer Inc.**

|                               |  |           |
|-------------------------------|--|-----------|
| Size<br>Custom                | Document Number<br><b>9 -- SKYPAKE 12/20 (RSV-1)</b> | Rev<br>1A |
| Date: Wednesday, May 20, 2015 | Sheet  | 9 of 42   |





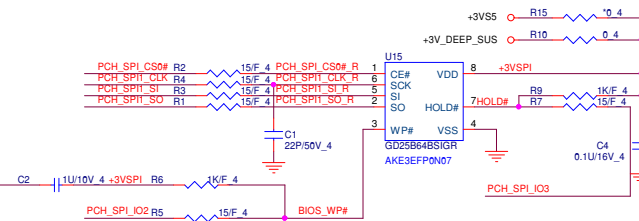
### 4M SPI ROM Socket



Need place to TOP



### SMBus/Pull-up(CLG)



R1/R2/R3/R4/R5/R7 close to U15 pin



**PROJECT : Y62P/Y63P**  
Quanta Computer Inc.

|                               |  |          |
|-------------------------------|--|----------|
| Size<br>Custom                | Document Number<br><b>10 -- SKYPAKE 14/20(SPI/LPC/SMBUS)</b> | Rev<br>1 |
| Date: Wednesday, May 20, 2015 | Sheet 1001   | 42       |

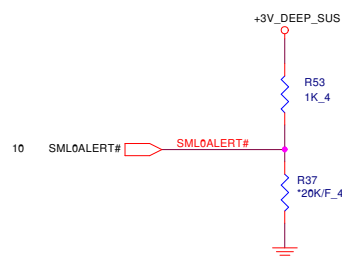
+3V\_DEEP\_SUS 4,10,12,14,15,16,18  
+3V 2,4,10,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39

# Functional Strap Definitions

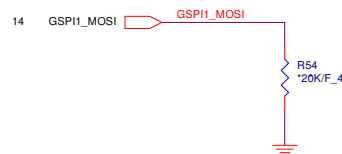
**DESIGN NOTE:**  
**WEAK PULL UP RESISTOR PRESENT ON THIS NET**



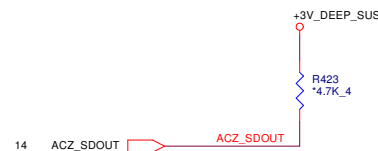
**TOP SWAP OVERRIDE**  
**HIGH - TOP SWAP ENABLE**  
**LOW-DISABLED**  
**HIGH: LPC SELECTED FOR SYSTEM FLASH**  
**WEAK INTERNAL PD**



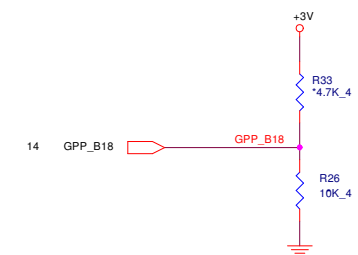
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



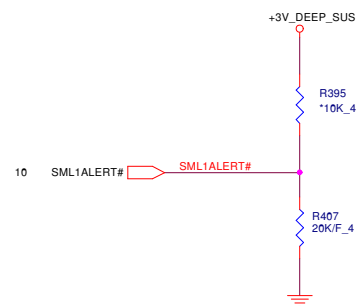
**No Boot:**  
The signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.  
**Bit 10      Boot BIOS Destination**  
0            SPI  
1            LPC



**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



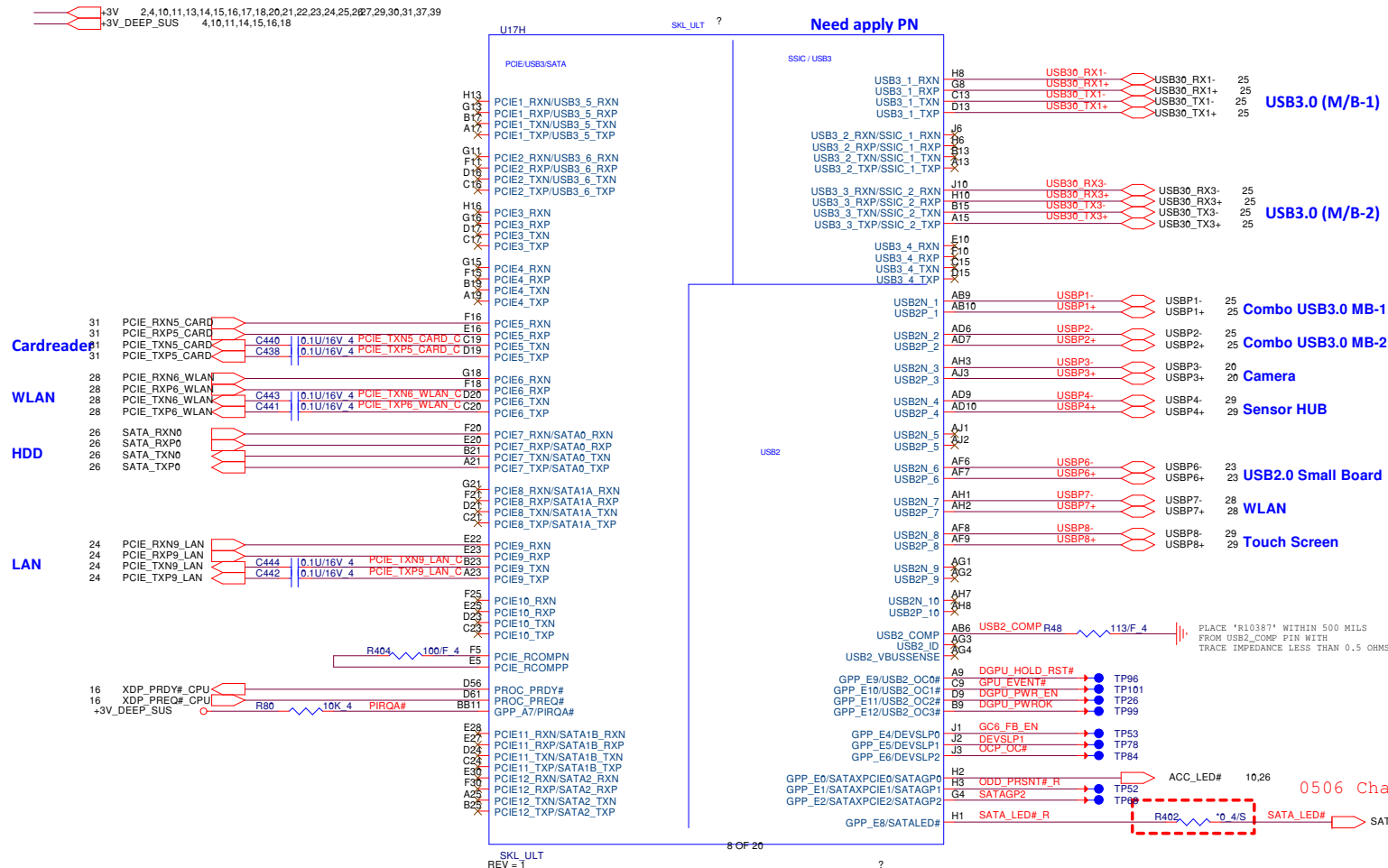
**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC is selected for EC.  
1 = eSPI is selected for EC.



**PROJECT : Y62P/Y63P**  
**Quanta Computer Inc.**

|                               |   |           |
|-------------------------------|---|-----------|
| Size<br>Custom                | Document Number<br><b>11 - SKYPAKE 15/20(HDA)</b> | Rev<br>1A |
| Date: Wednesday, May 20, 2015 | Sheet   | 11 of 42  |

+3V 2,4,10,11,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39  
 +3V\_DEEP\_SUS 4,10,11,14,15,16,18



PCI-E Port Mapping Table

| PCI-E Port | Function   | CLK RQ Port | Function   |
|------------|------------|-------------|------------|
| Port1      | Un-used    | Port0       | Un-used    |
| Port2      | Un-used    | Port1       | CardReader |
| Port3      | Un-used    | Port2       | WLAN       |
| Port4      | Un-used    | Port3       | LAN        |
| Port5      | CardReader | Port4       | Un-used    |
| Port6      | WLAN       | Port5       | Un-used    |
| Port7      | HDD        |             |            |
| Port8      | Un-used    |             |            |
| Port9      | LAN        |             |            |
| Port10     | Un-used    |             |            |

USB3.0 Port Mapping Table

| USB3.0 | Function    |
|--------|-------------|
| PORT-1 | USB3.0 MB-1 |
| PORT-2 | NC          |
| PORT-3 | USB3.0 MB-2 |
| PORT-4 | NC          |

USB2.0 Port Mapping Table

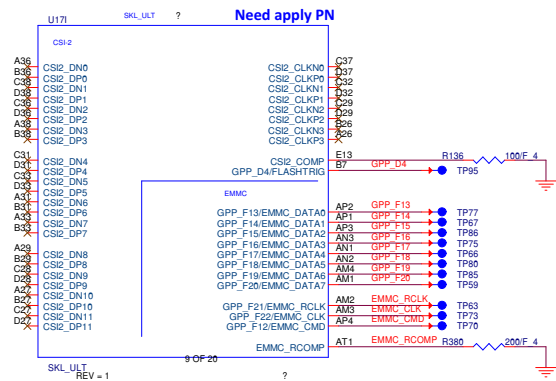
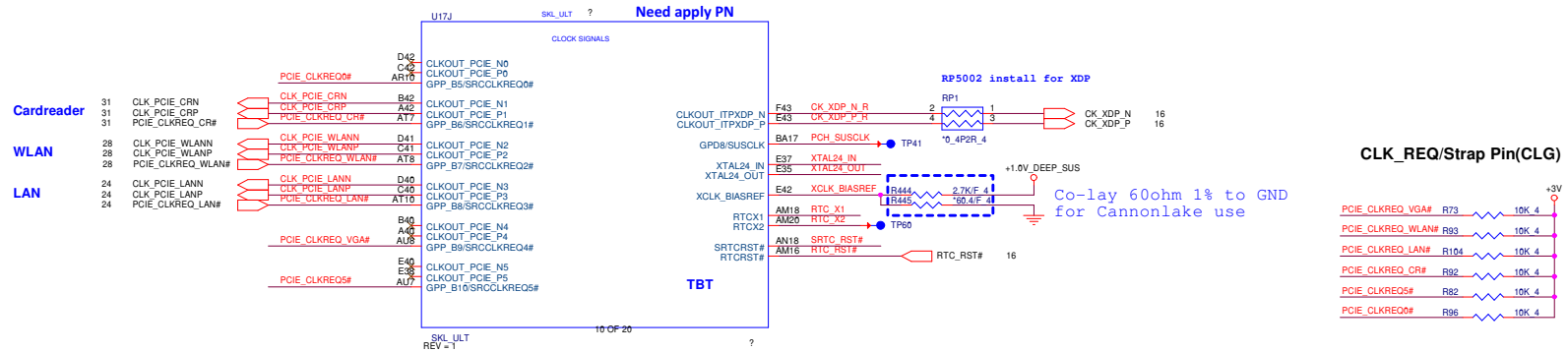
| USB2.0  | Function           |
|---------|--------------------|
| PORT-1  | Cobime USB3.0 MB-1 |
| PORT-2  | Cobime USB3.0 MB-2 |
| PORT-3  | Camera             |
| PORT-4  | Sensor HUB         |
| PORT-5  | NC                 |
| PORT-6  | USB2.0 Small Board |
| PORT-7  | WLAN               |
| PORT-8  | Touch Screen       |
| PORT-9  | NC                 |
| PORT-10 | NC                 |



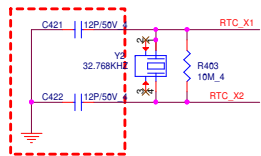
**PROJECT : Y62P/Y63P**  
**Quanta Computer Inc.**

Size Custom Document Number 12 - SKYPAKE 16/20 (PCIE/USB) Rev 1A  
 Date: Wednesday, May 20, 2015 Sheet 12 of 42

|                |  |
|----------------|--|
| +3V_RTC_2      | 4,15   |
| +3V_RTC        | 4,15,27,28,32  |
| +3V            | 2,4,10,11,12,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39 |
| +1.0V_DEEP_SUS | 9,15,16,35,36  |

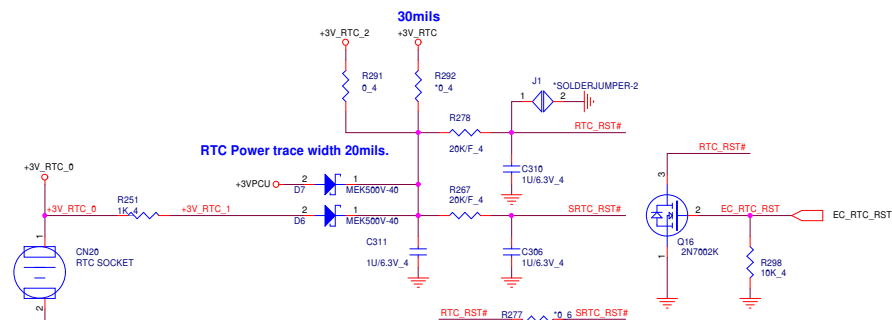


**RTC Clock 32.768KHz**



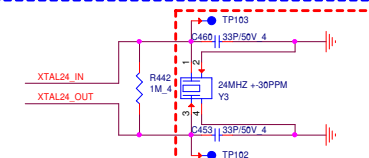
0506 Change C421, C422 from 18P to 12P  
for vendor suggest

## RTC Circuitry(RTC)



## External Crystal and Green Clock

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.



0512 Change Y3 from BG624000044 to BG6240000107  
0512 Change C456, C460 from 12pF to 22pF  
0514 Change C456, C460 from 22pF to 27pF  
0520 Change C456, C460 from 27pF to 33pF



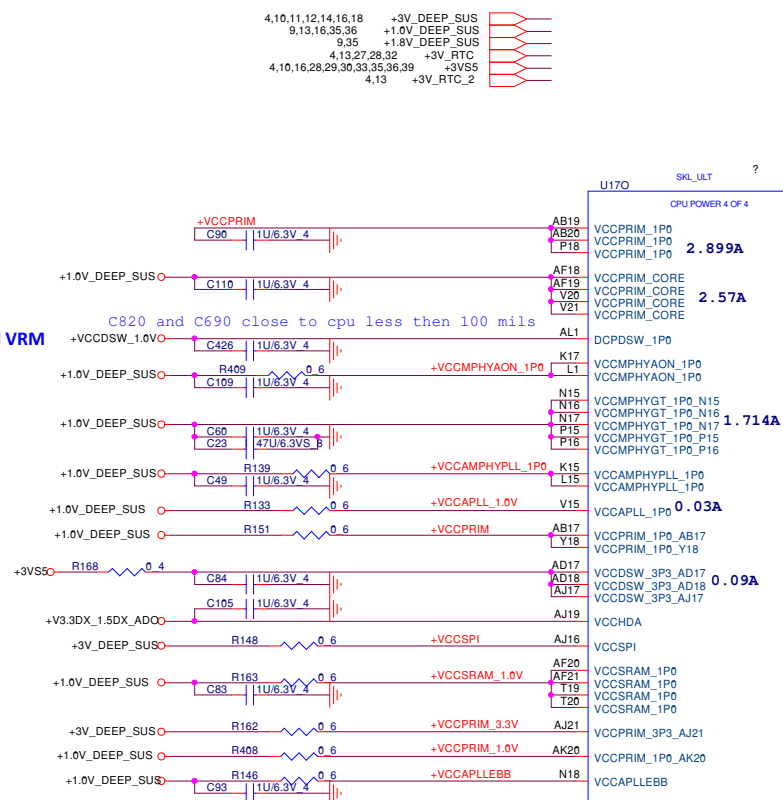
**PROJECT : Y62P/Y63P**  
Quanta Computer Inc.

|                               |   |        |
|-------------------------------|---|--------|
| Size Custom                   | Document Number<br><b>13 -- SKYPAKE 17/20 (CLK)</b> | Rev 1A |
| Date: Wednesday, May 20, 2015 | Sheet 13 of   | 42     |

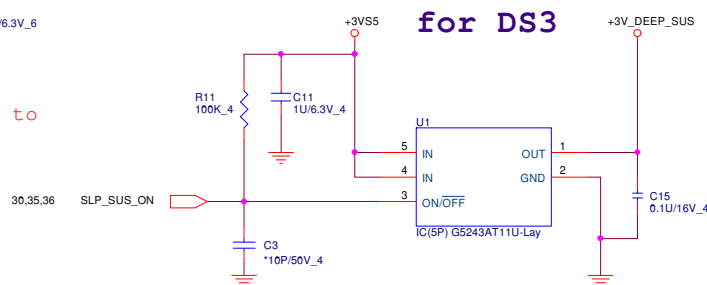
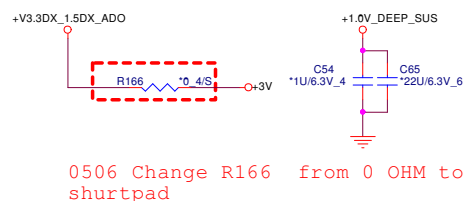




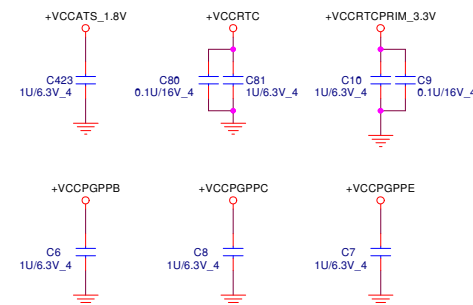
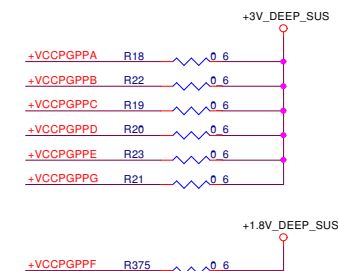
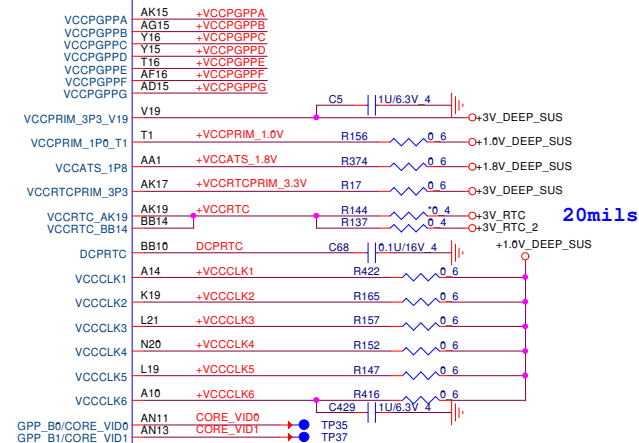
PCH Internal VRM

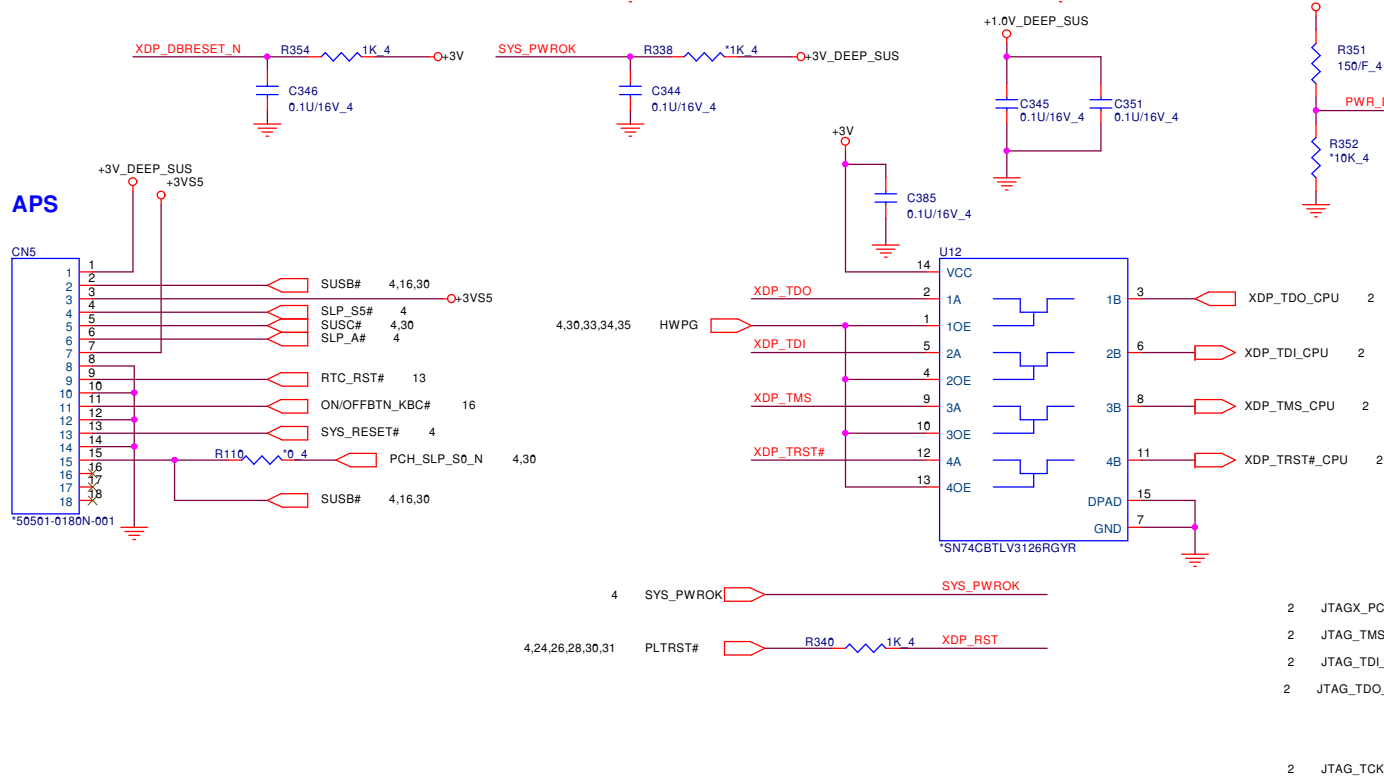
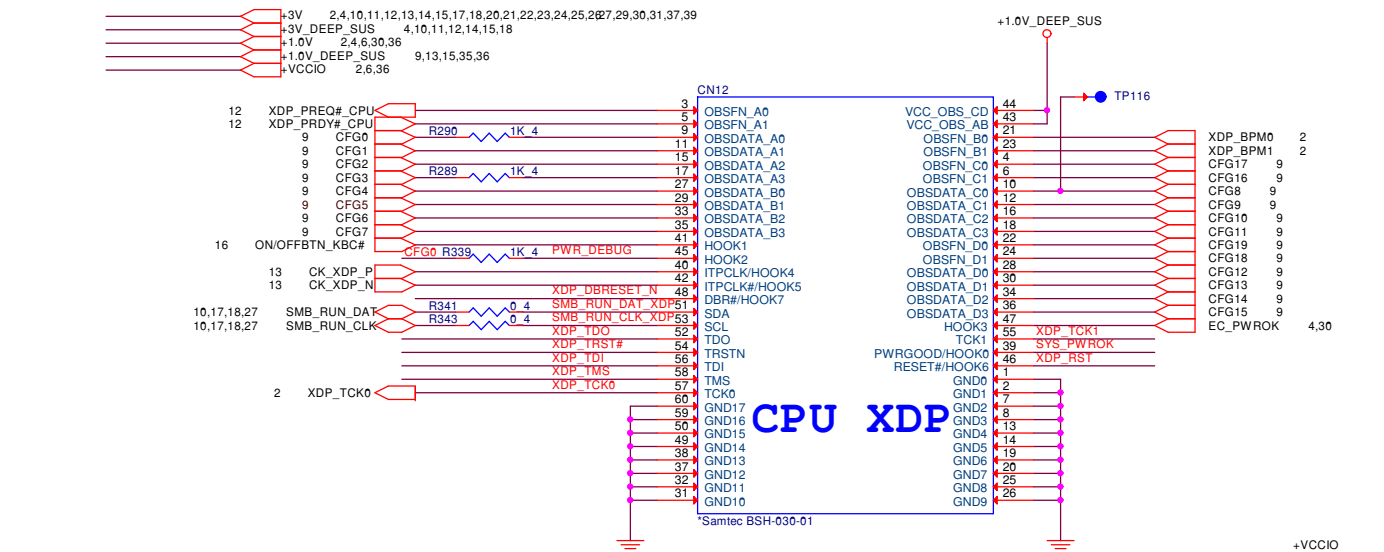


for DS3



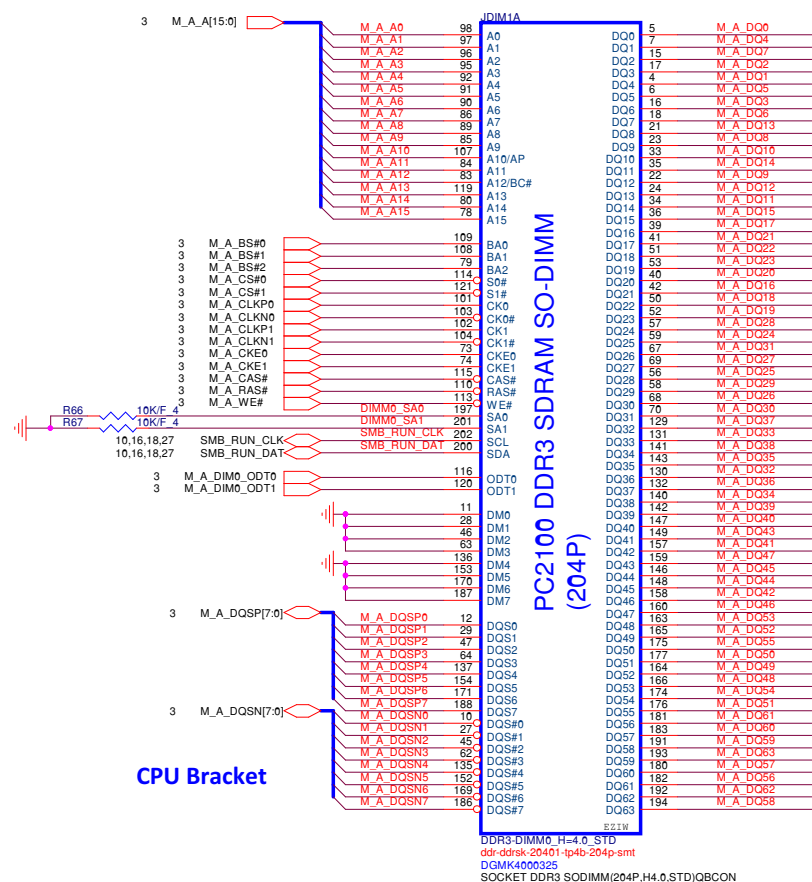
Need apply PN





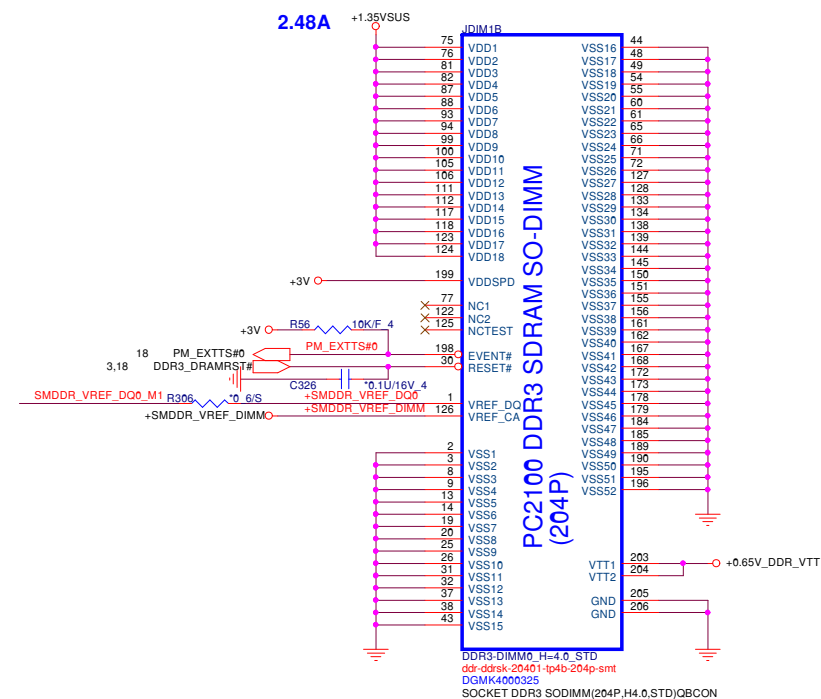
**PROJECT : Y62P/Y63P**  
Quanta Computer Inc.

|                               |   |           |
|-------------------------------|---|-----------|
| Size                          | Document Number<br><b>16 -- HSW XDP &amp; APS</b> | Rev<br>1A |
| Date: Wednesday, May 20, 2015 | Sheet 16 of 42                                    |           |



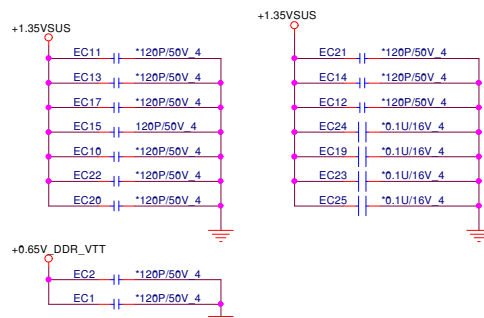
CPU Bracket

M\_A\_DQ[63:0] 3



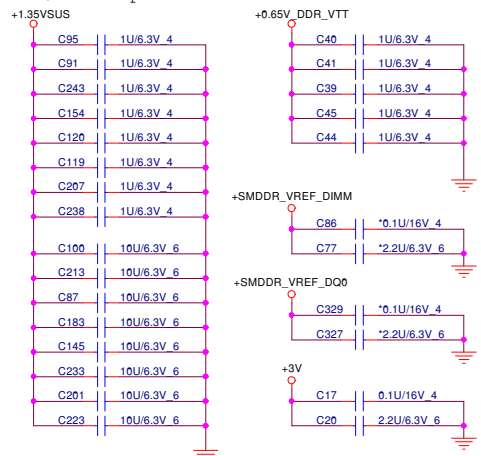
2,4,10,11,12,13,14,15,16,18,20,21,22,23,24,25,26,27,29,30,31,37,39 +3V  
3,6,18,34,36 +1.35VSUS  
18,34 +0.65V\_DDR\_VTT  
18 +SMDDR\_VREF\_DIMM

## For EMI RESERVE

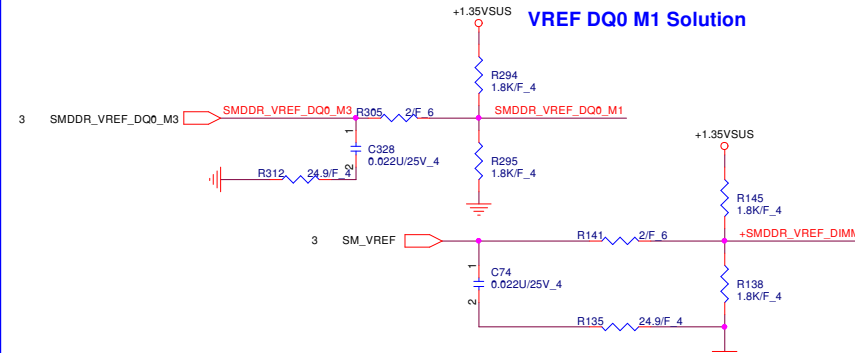


## Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector

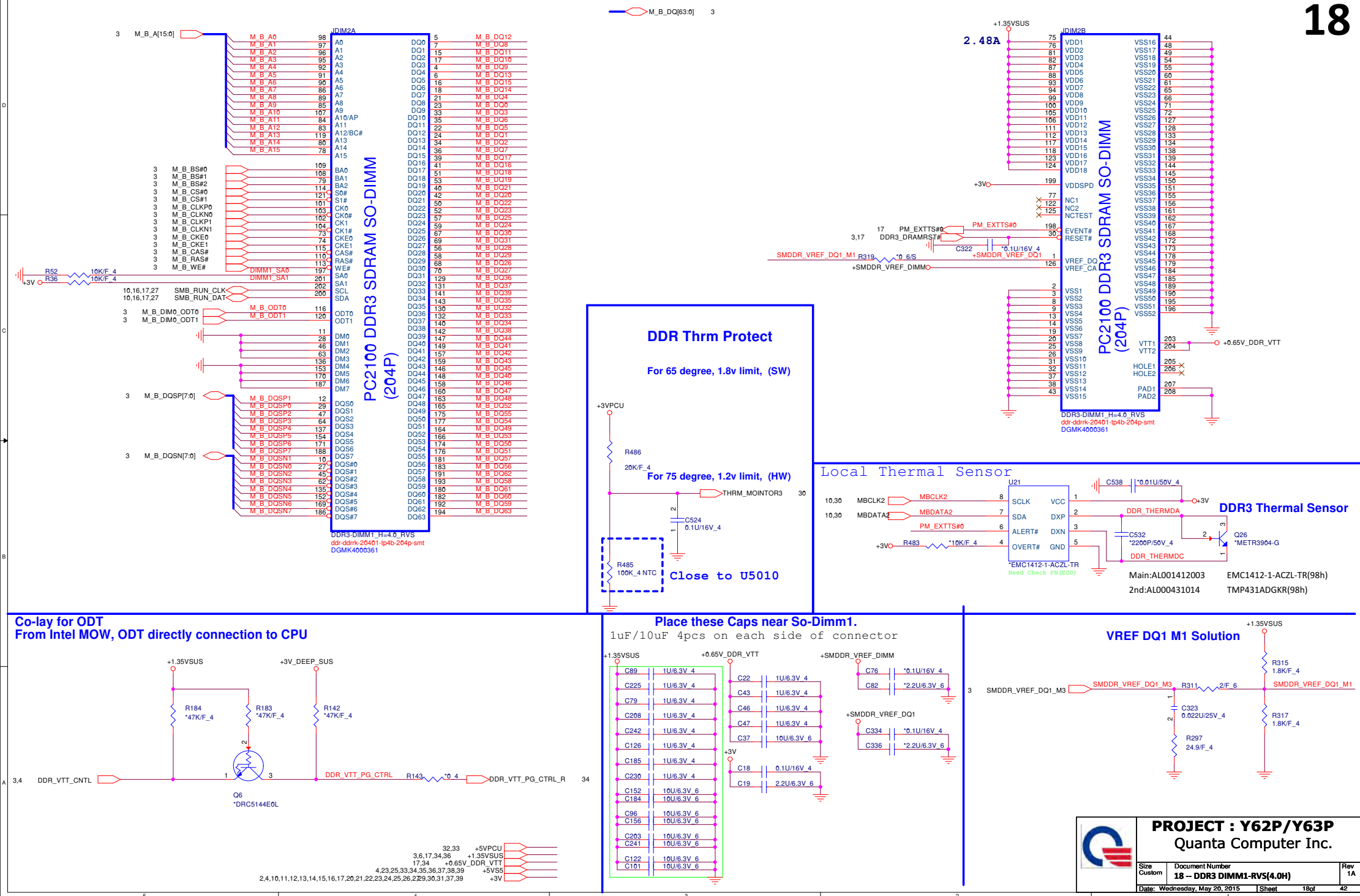


## VREF DQ0 M1 Solution



**PROJECT : Y62P/Y63P**  
**Quanta Computer Inc.**

| Size   | Document Number            | Rev            |
|--------|----------------------------|----------------|
| Custom | 17 -- DDR3 DIMM0-STD(4.0H) | 1A             |
| Date:  | Wednesday, May 20, 2015    | Sheet 17 of 42 |



D

D

C


C

B

B

A

A

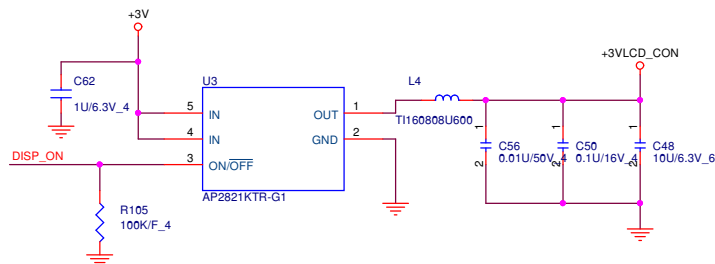
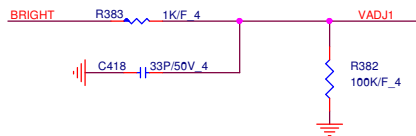
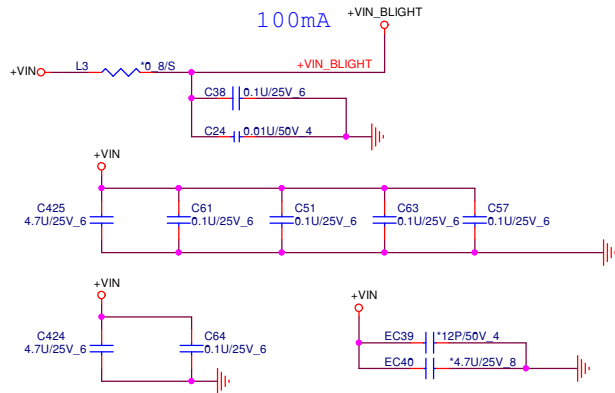
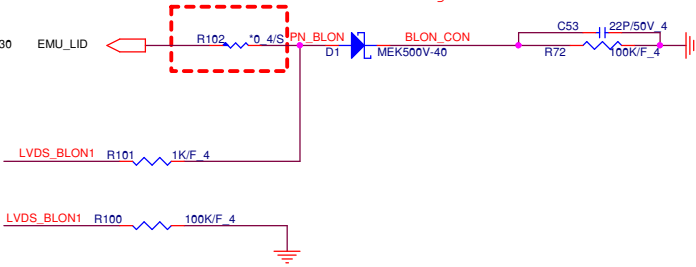


**PROJECT : Y62P/Y63P**  
**Quanta Computer Inc.**

|                               |                                   |                |
|-------------------------------|-----------------------------------|----------------|
| Size<br>Custom                | Document Number<br><b>RTD2136</b> | Rev<br>1A      |
| Date: Wednesday, May 20, 2015 |                                   | Sheet 19 of 42 |

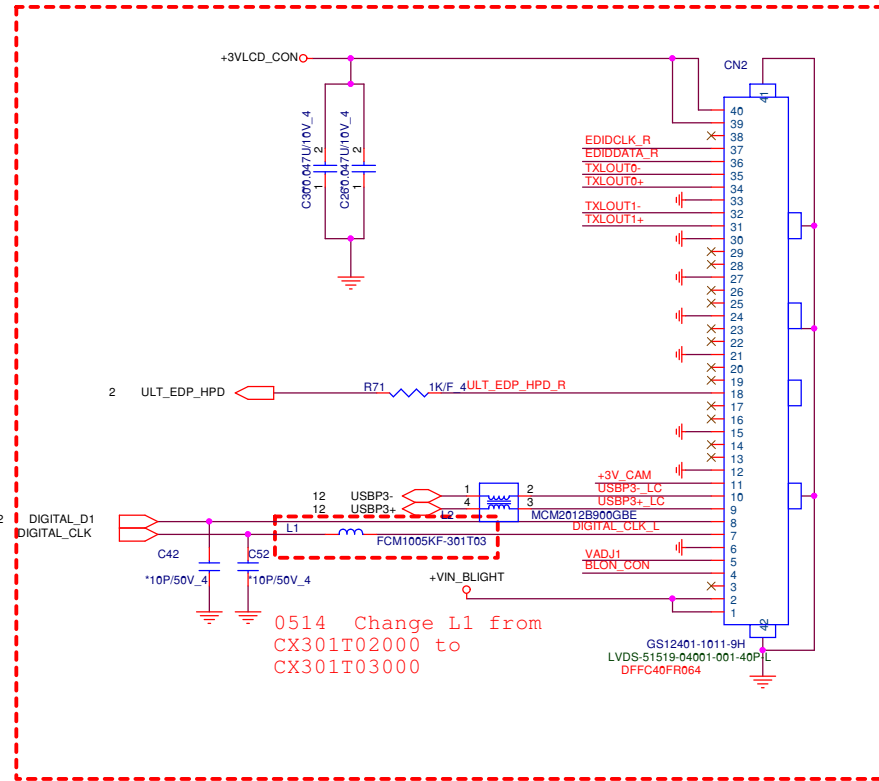
# LID Switch

0506 Change R102 from 0 OHM to shurtpad



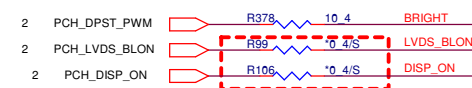
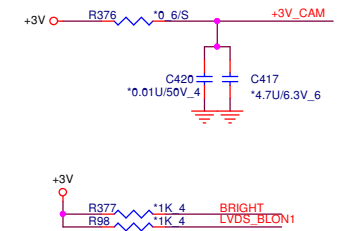
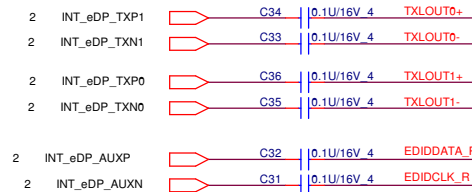
eDP Conn.

20

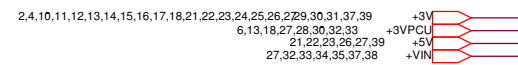


0514 Change L1 from CX301T02000 to CX301T03000

0506 Change CN2 footprint from lvds-50671-04041-00140p-1 to LVDS-51519-04001-001-40P-L



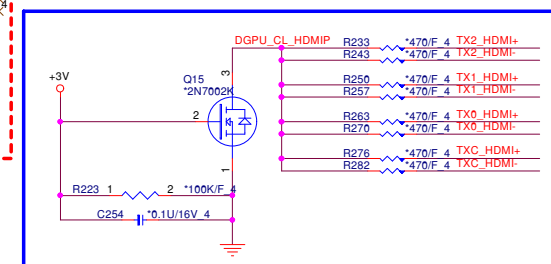
0506 Change R99, R106 from 0 OHM to shurtpad



**PROJECT : Y62P/Y63P**  
Quanta Computer Inc.

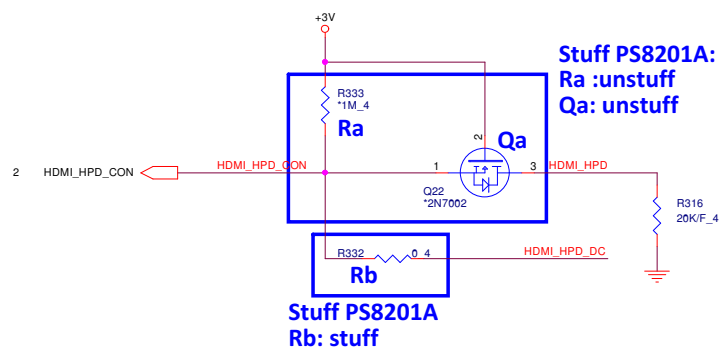
|                               |                 |        |
|-------------------------------|-----------------|--------|
| Size Custom                   | Document Number | Rev 1A |
| LCD CONN/LID/CAM              |                 |        |
| Date: Wednesday, May 20, 2015 | Sheet 20 of 42  |        |





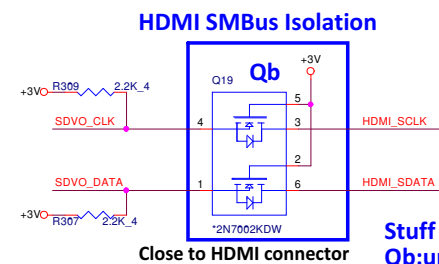
## Stuff PS8201A:

### DEL ALL



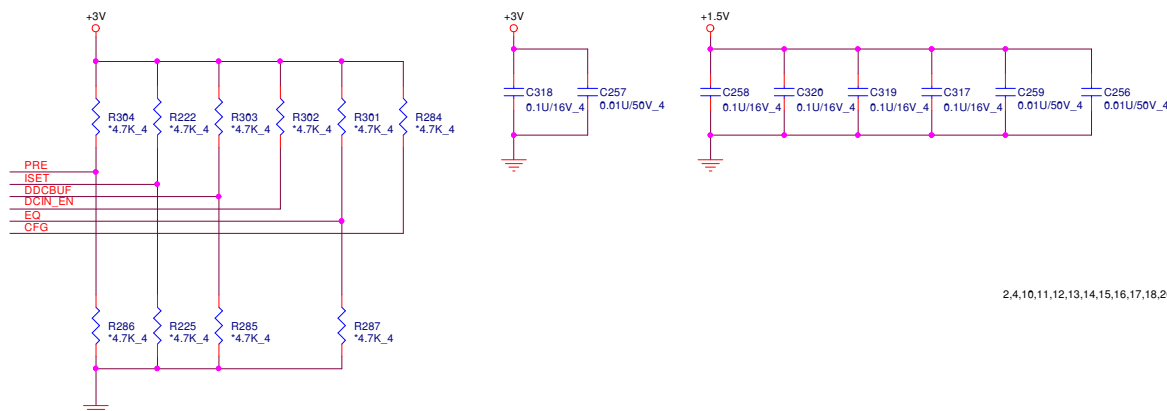
Stuff PS8201A:  
Ra :unstuff  
Qa: unstuff

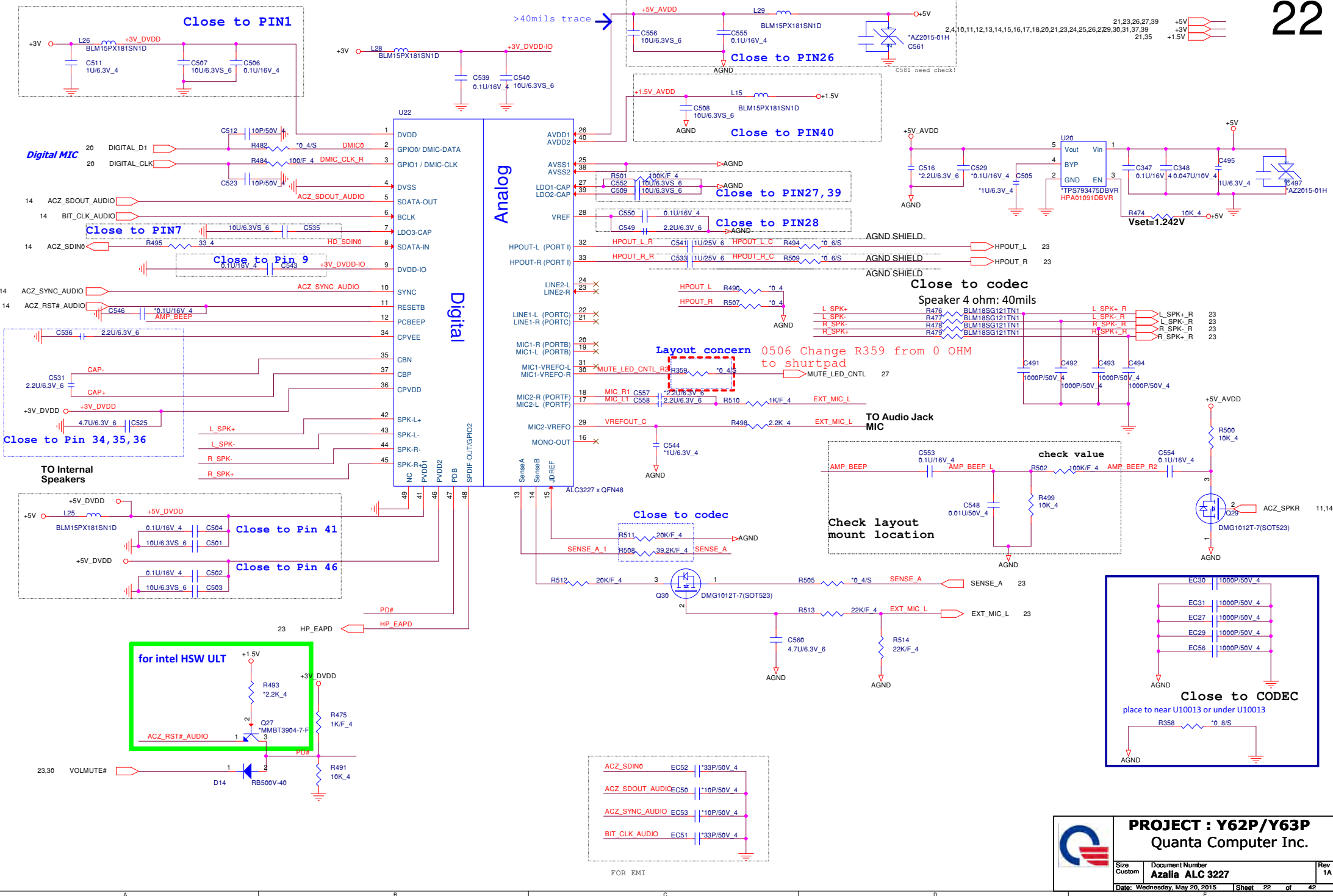
Stuff PS8201A  
Rb: stuff



## HDMI SMBus Isolation

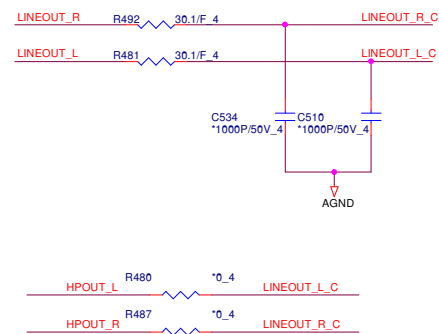
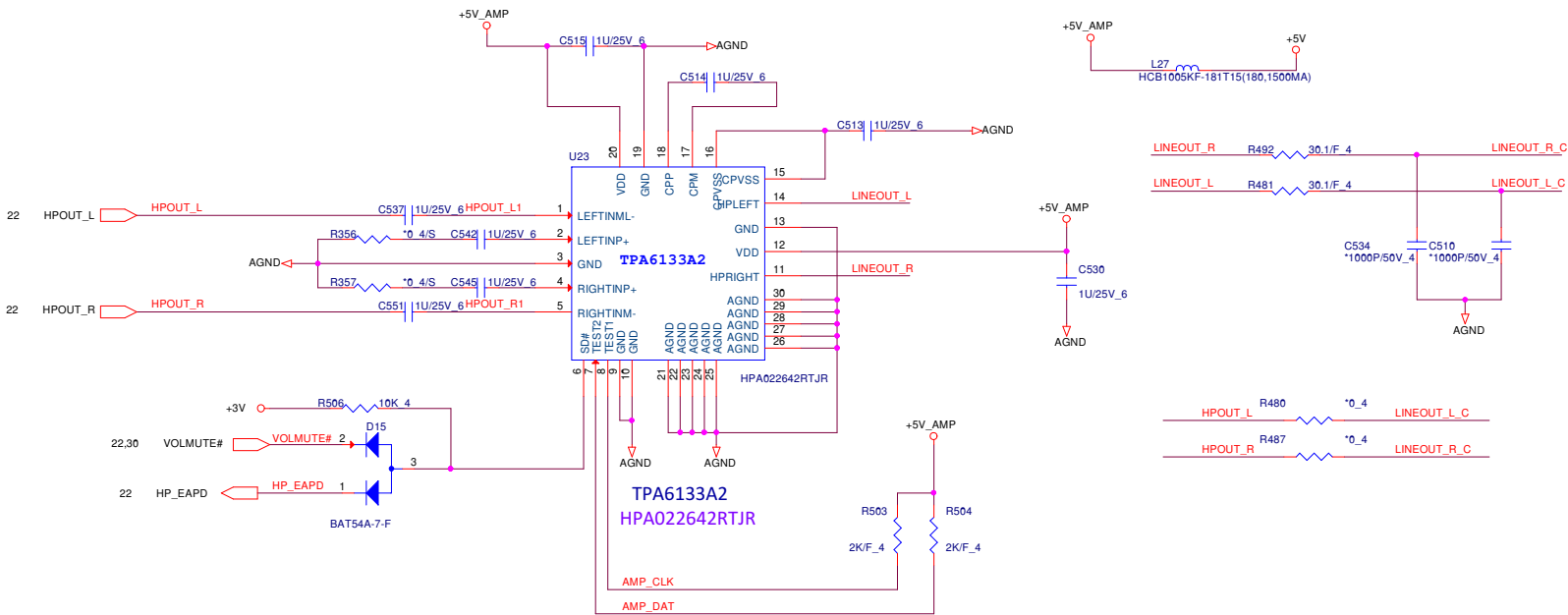
Stuff PS8201A:  
Ob:unstuff



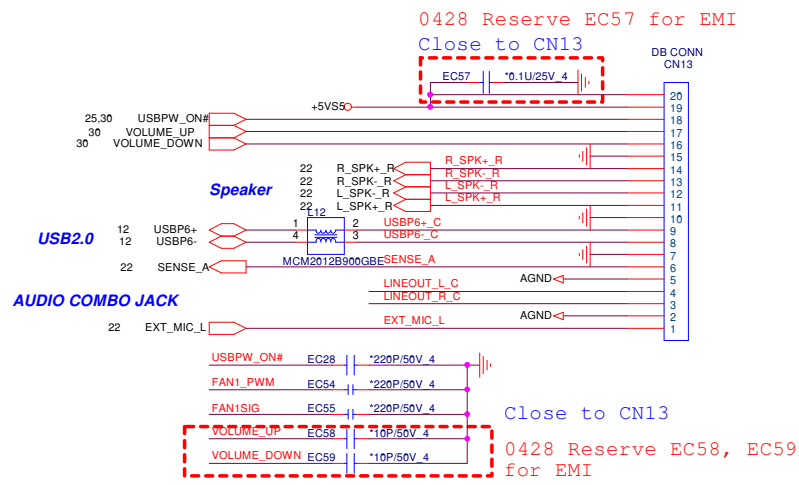


# Head Phone out

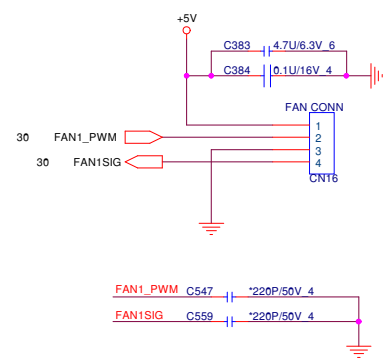
23



## Audio Board



## FAN

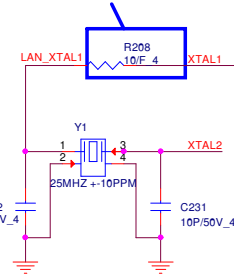


2,4,10,11,12,13,14,15,16,17,18,20,21,22,24,25,26,2Z9,30,31,37,39  
21,22,26,27,39  
4,25,33,34,35,36,37,38,39

+3V  
+5V  
+5VSS

|                               |                             |   |
|-------------------------------|-----------------------------|---|
|                               | <b>PROJECT : Y62P/Y63P</b>  |   |
|                               | <b>Quanta Computer Inc.</b> |   |
|                               | Size Custom                 | Document Number<br><b>Audio/AMP HPA022642RTJR</b> |
| Date: Wednesday, May 20, 2015 |                             | Sheet 23 of 42                                    |

For EMI 0 ~ 22 ohm

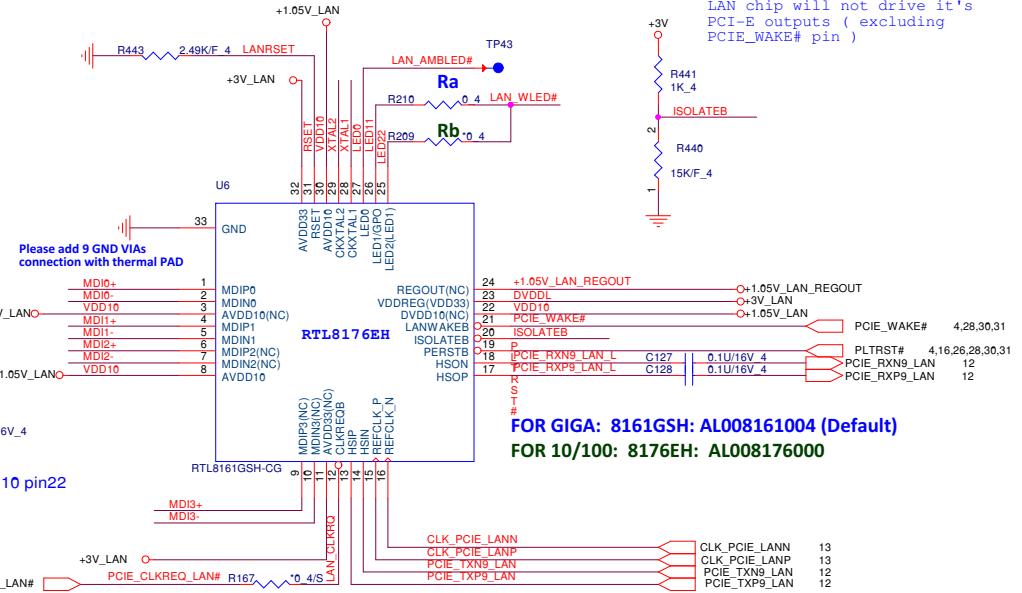


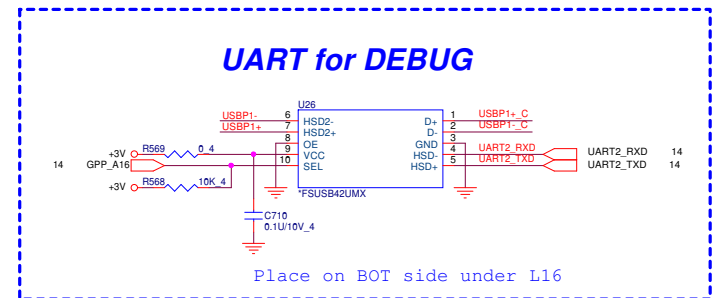
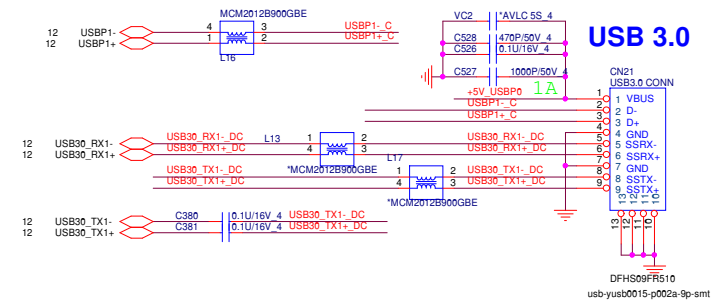
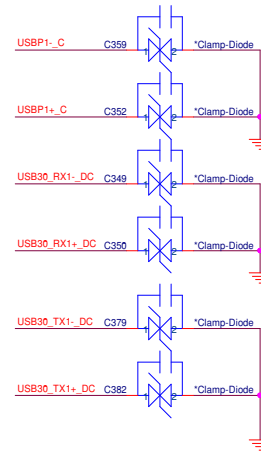
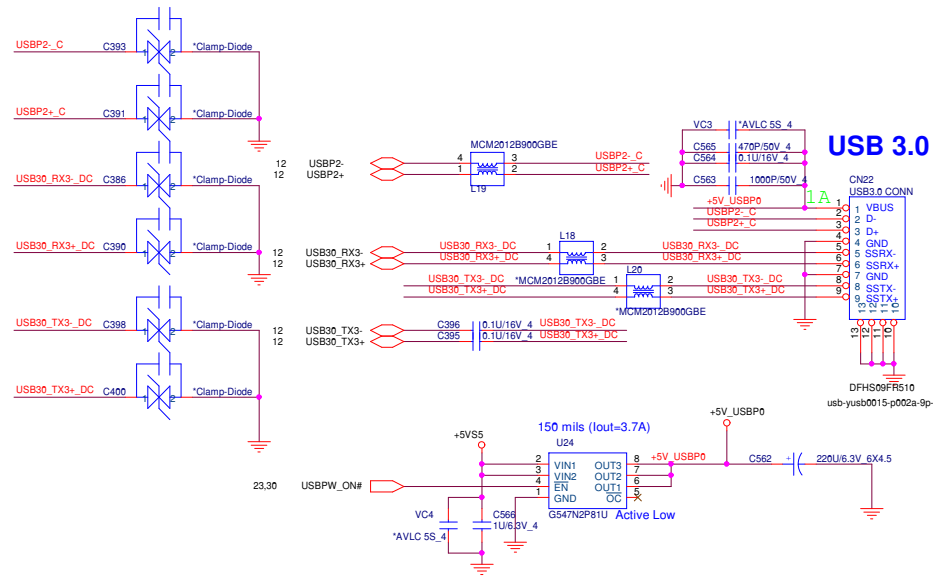
LED1:

FOR GIGA 8161: Stuff Ra, DEL Rb (Default)

FOR 10/100 8176: Stuff Rb, DEL Ra

if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs ( excluding PCIE\_WAKE# pin )

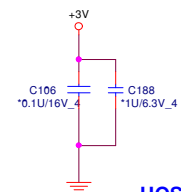
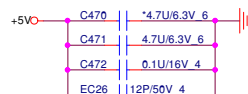
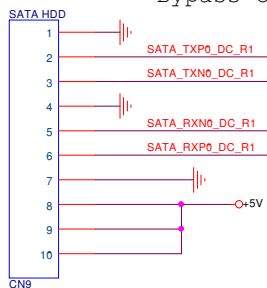




4.23,33,34,35,36,37,38,39  
2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,26,27,29,30,31,37,39

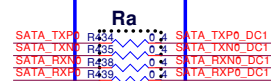
### SATA HDD Connector(Cable type)

Bypass CAP close conn

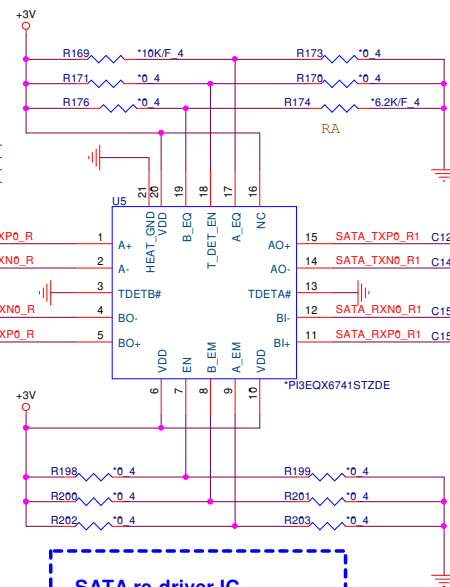
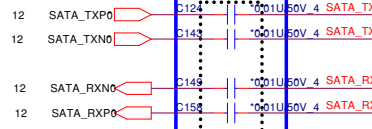


## ***SATA Re-driver***

**Ra & Rb need place close**

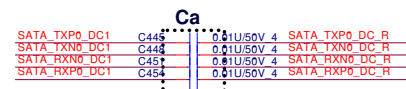


HOST



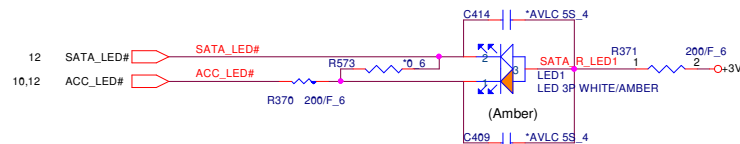
SATA re-driver IC  
stuff Rb,Cb , unstuff Ra,Ca

unstuff SATA re-driver IC  
stuff Ra,Ca , unstuff Rb,Cb



|              |                             |                          |
|--------------|-----------------------------|--------------------------|
| LED1         | PN                          |                          |
| Dual Color   | <a href="#">BEWY0009ZA0</a> | stuff R370, unstuff R573 |
| Single Color | <a href="#">BEWH0046Z00</a> | stuff R573, unstuff R370 |

**SATA LED**

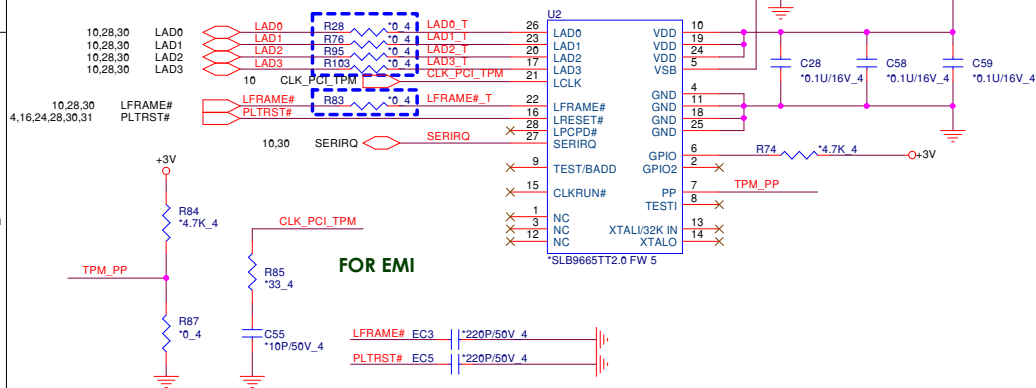


## TPM (2.0)

Address

|             |                         |
|-------------|-------------------------|
|             | <b>BADD</b>             |
| <b>HIGH</b> | <b>4EH/4F</b> (default) |

Close to EC Side



2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,27,29,30,31,37,39  
21,22,23,27,31



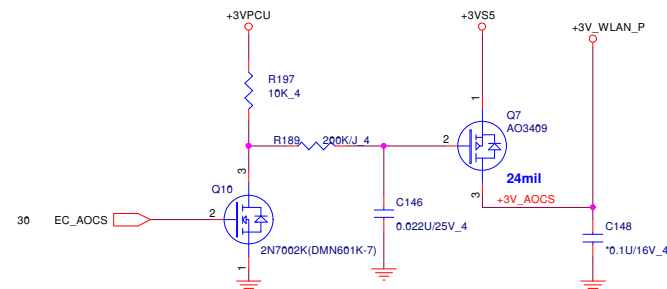
**PROJECT : Y62P/Y63P**  
Quanta Computer Inc.

|                               |   |           |
|-------------------------------|---|-----------|
| Size<br>Custom                | Document Number<br><b>HDD/mSATA/FAN/LED</b> | Rev<br>1A |
| Date: Wednesday, May 20, 2015 | Sheet 26 of 42                              |           |

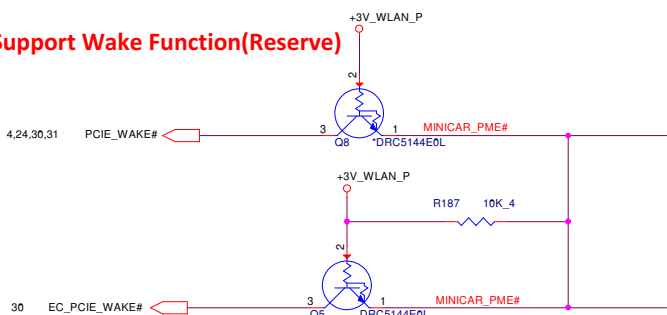


|                               |  |                |
|-------------------------------|--|----------------|
| Size<br>Custom                | Document Number<br><b>PB/TP/KB/FAN/EMI Cap</b> | Rev<br>1A      |
| Date: Wednesday, May 20, 2015 |  | Sheet 27 of 42 |

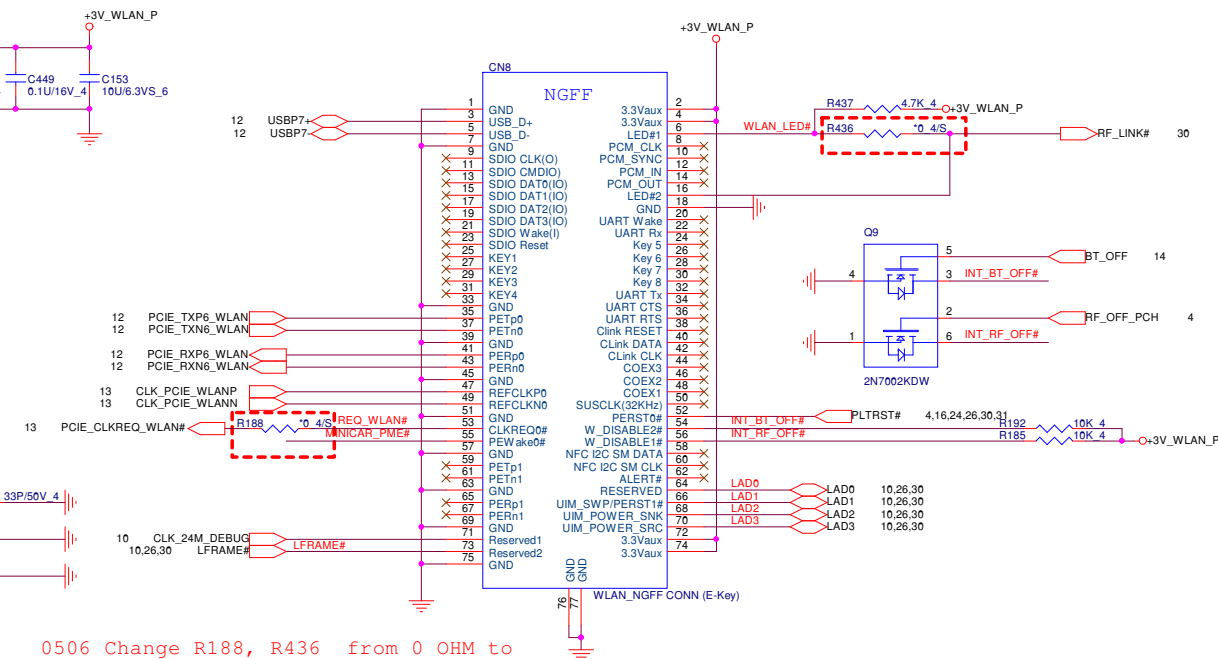
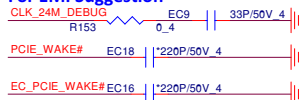
# Mini Card WLAN/BT(Optional)



## Support Wake Function(Reserve)

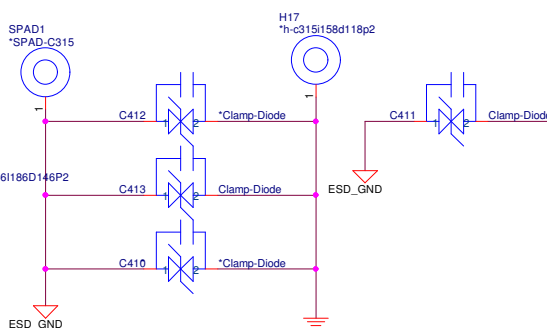
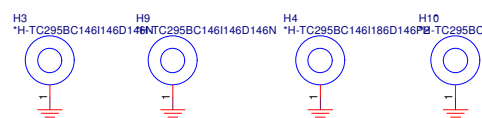
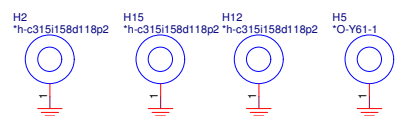
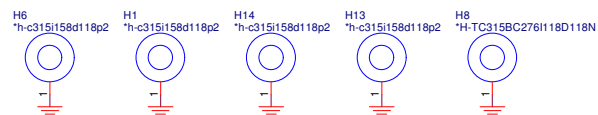


## For EMI Suggestion

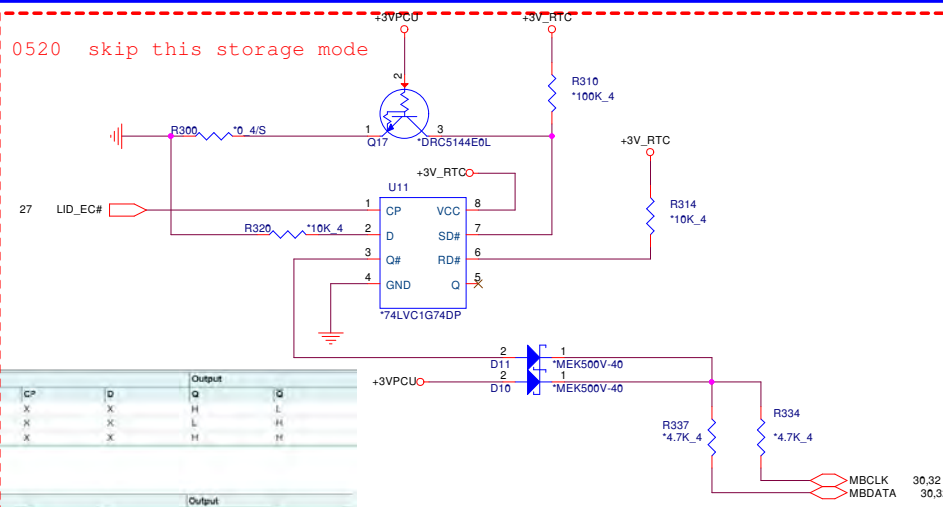


0506 Change R188, R436 from 0 OHM to shurtpad

## Hole



0520 skip this storage mode



| Input | Rd | CP | D | Q | Q |
|-------|----|----|---|---|---|
| SD    | H  | X  | X | H | L |
| H     | L  | X  | X | L | H |
| L     | L  | X  | X | H | H |

| Input | Rd | CP | D | Q | Q |
|-------|----|----|---|---|---|
| SD    | H  | T  | L | L | H |
| H     | H  | T  | H | H | L |

(1) H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
T = LOW-to-HIGH or HIGH-to-LOW transition;  
Q<sub>new</sub> = state after the next LOW-to-HIGH or HIGH-to-LOW transition.

4,10,15,16,29,30,33,35,36,39  
27 +3V\_WLAN\_P  
4,13,15,27,32 +3V\_RTC  
2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39 +3V  
21,22,23,26,27,39 +5V  
6,13,16,27,30,32,33 +3VPCU



**PROJECT : Y62P/Y63P**  
**Quanta Computer Inc.**

| Size                          | Document Number        | Rev |
|-------------------------------|------------------------|-----|
| Custom                        | WLAN/G-Sensor/G-CLK/TS | 1A  |
| Date: Wednesday, May 20, 2015 | Sheet 28 of 42         |     |

20MIL

+3V

10MIL (For PLL Power)

Close to CN3

Close to U23

***Close to U9***

To Sensor Hub SMBUS

Close to U23

IT8350E  
LQFP-48

Reserved TX/RX for debugging

```
if no use ADC function,  
please pull down to GND  
SMINTx for sensor interrupt
```

GPG2 can't floating

External crystal is must be item  
when USB func. is used !

32.768kHz clock lines:

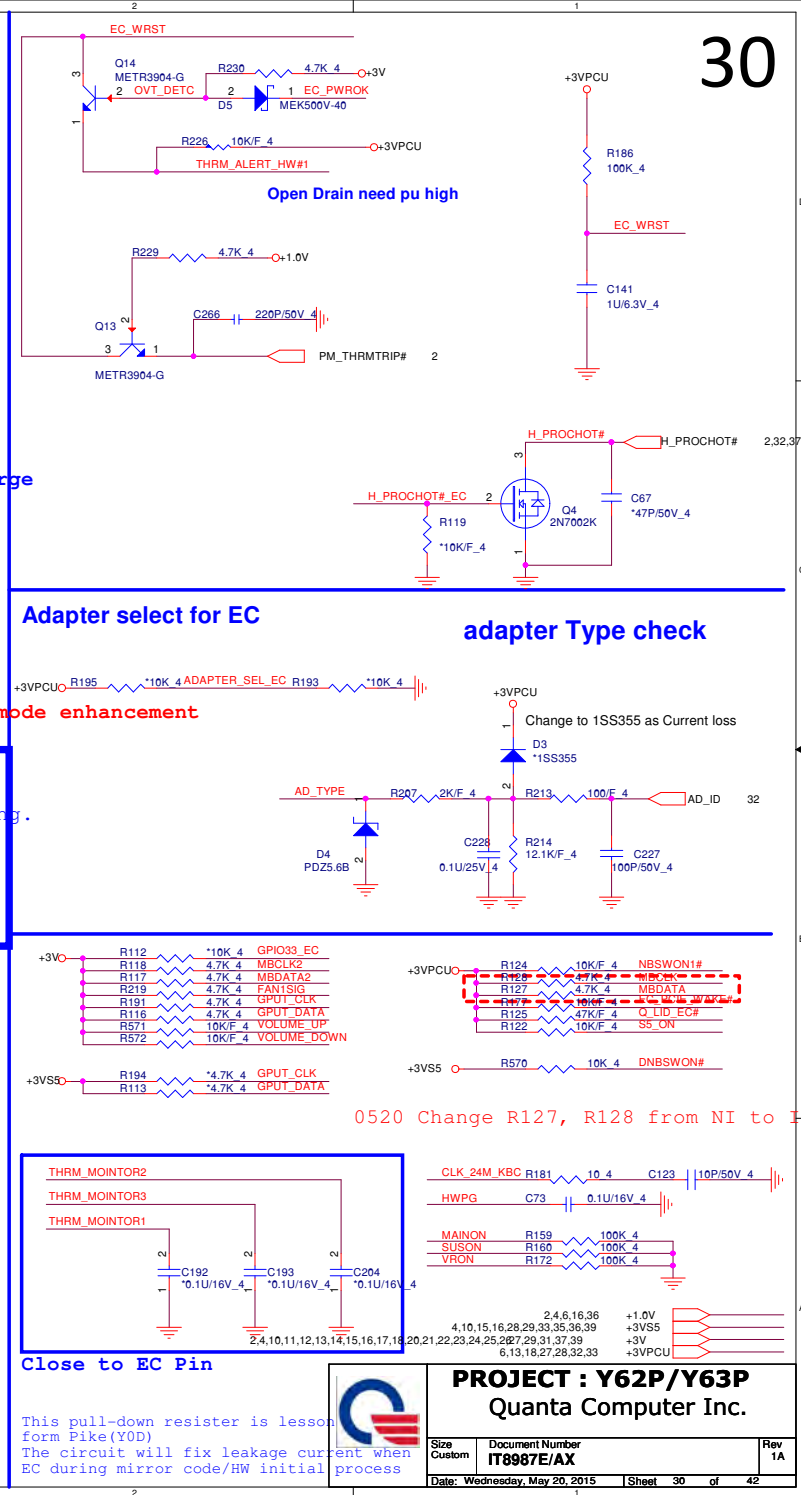
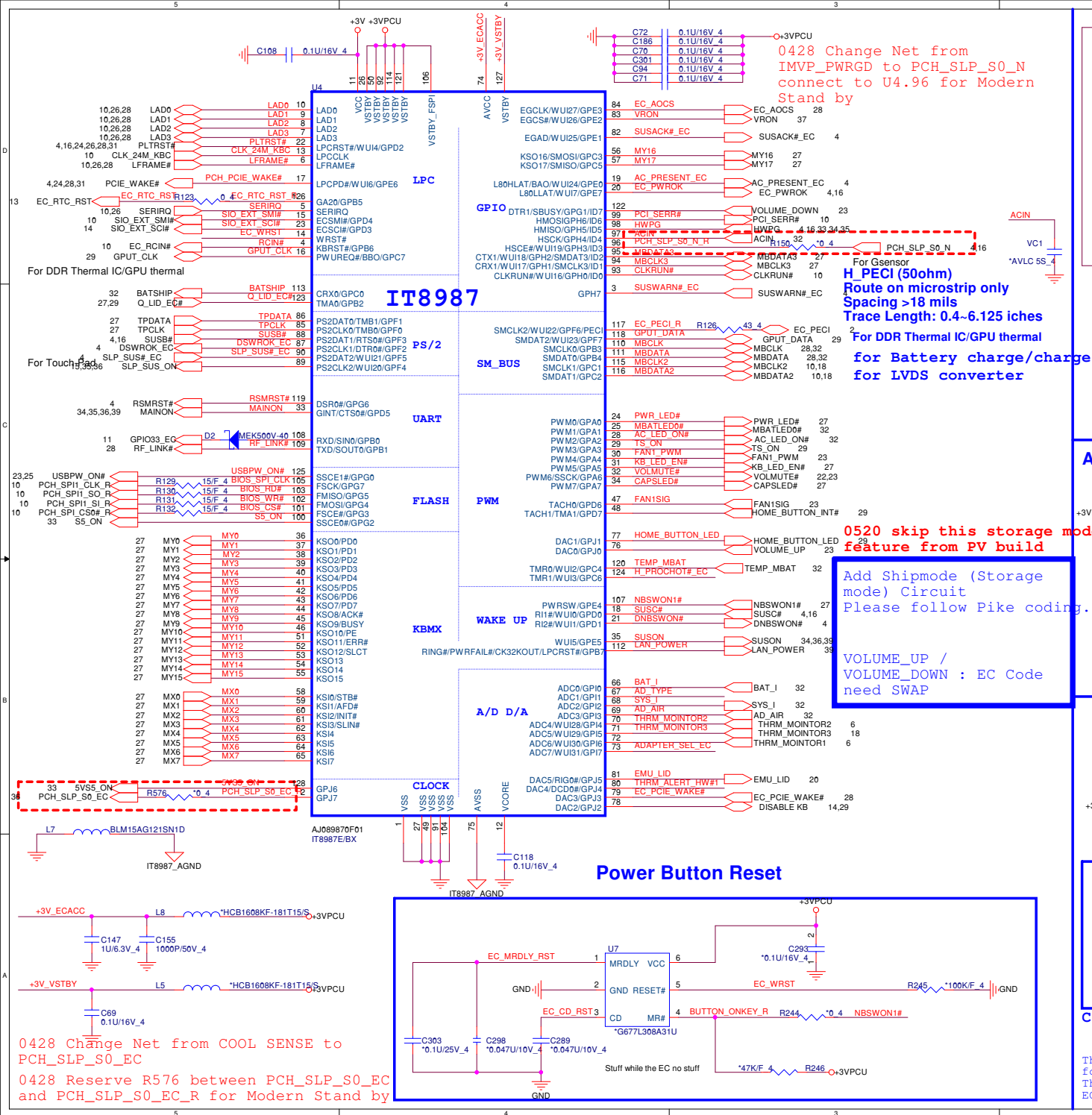
- a. If possible, please avoid using any through-hole
- b. Please make the trace length short, and the trace width wide enough.
- c. The spacing to the closest neighbor should be wide enough.

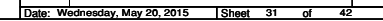
0415 Del TS Co-Lav CN6

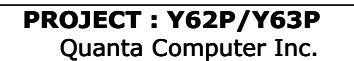
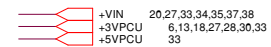


**PROJECT : Y62P/Y63P**  
Quanta Computer Inc.

|                               |   |                |
|-------------------------------|---|----------------|
| Size Custom                   | Document Number<br><b>ITE8350/HP9DS0/HP3DC2</b> | Rev<br>1.      |
| Date: Wednesday, May 20, 2015 |   | Sheet 29 of 42 |







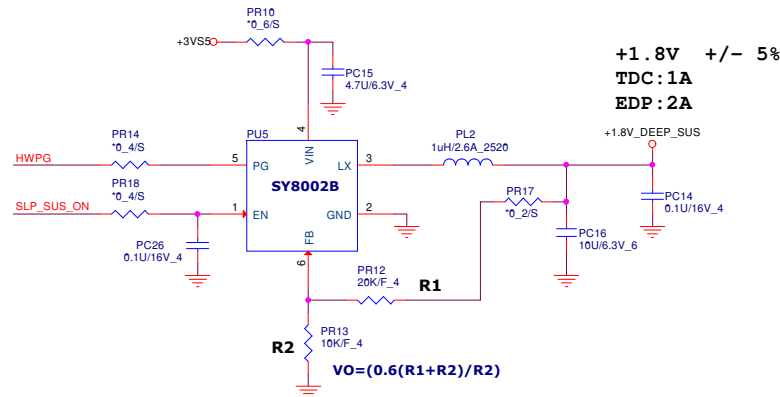
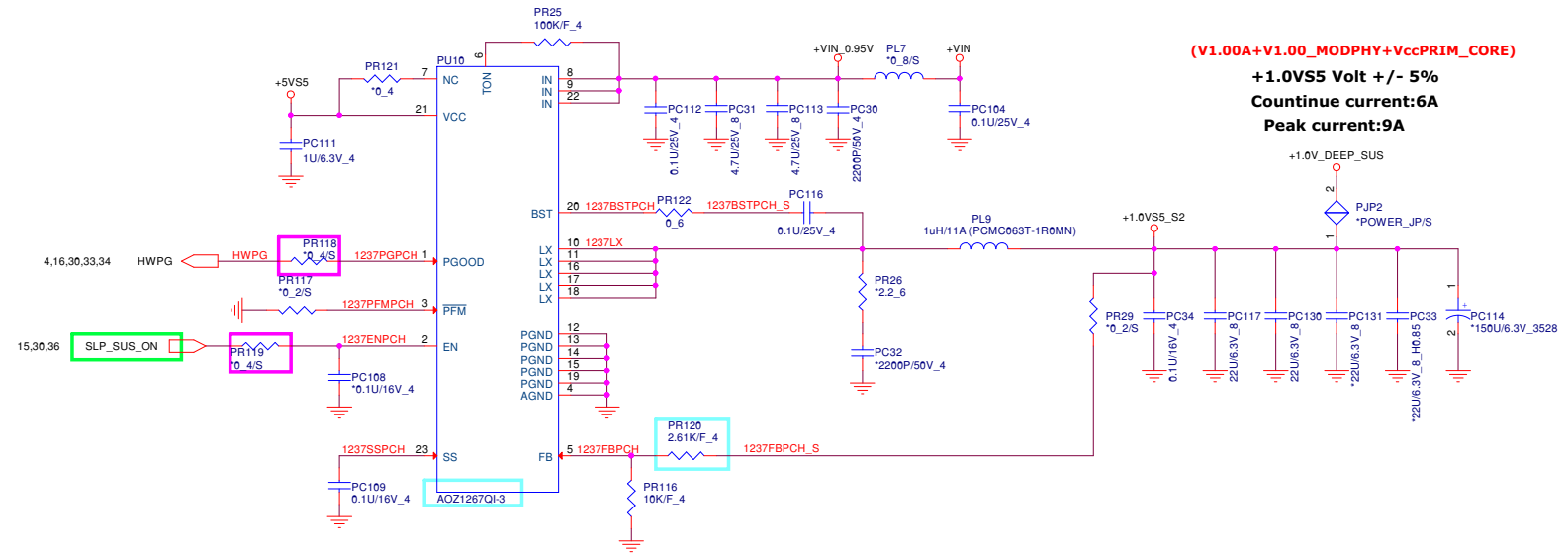
Date: Wednesday, May 20, 2015 Sheet 32 of 42



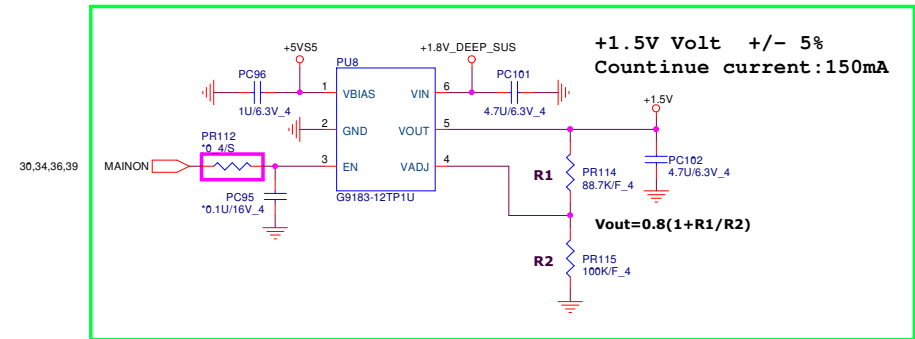




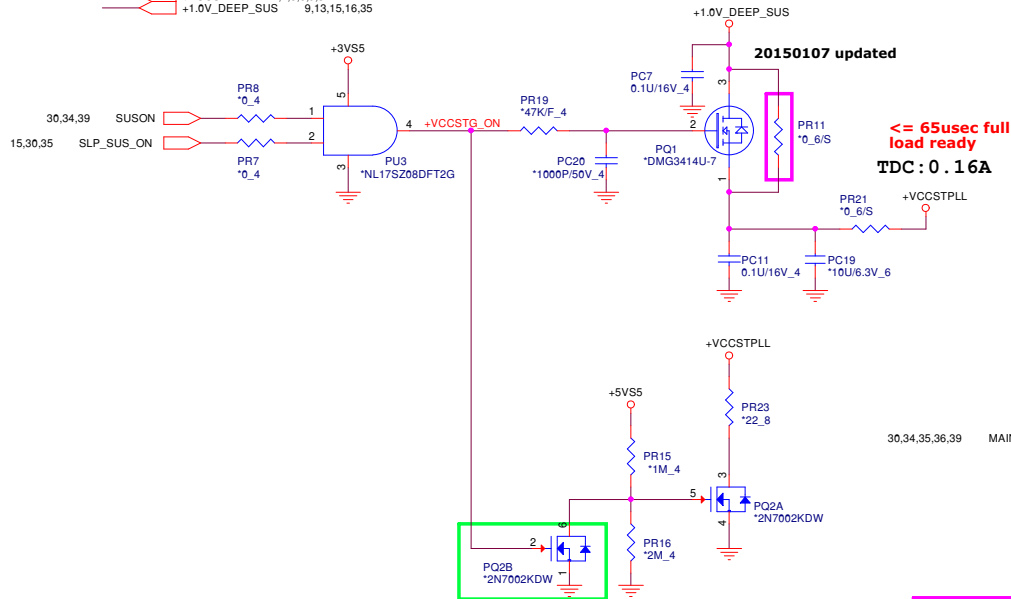
+VIN 20,27,32,33,34,37,38  
 +3VS5 4,10,15,16,28,29,30,33,36,39  
 +5VS5 4,23,25,33,34,36,37,38,39  
 +1.0V\_DEEP\_SUS 9,13,15,16,36  
 +1.8V\_DEEP\_SUS 9,15



20150111 updated

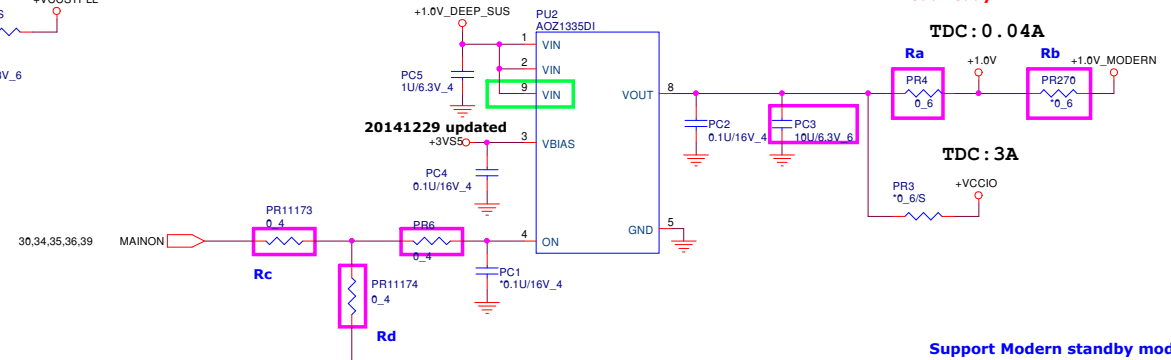


|                |                              |
|----------------|------------------------------|
| +1.0V          | 2,4,6,16,30                  |
| +3VS5          | 4,10,15,16,28,29,30,33,35,39 |
| +5VS5          | 4,23,25,33,34,35,37,38,39    |
| +VCCIO         | 2,6,16                       |
| +VCCSTPLL      | 2,4,5,6,9,37                 |
| +1.0V_DEEP_SUS | 9,13,15,16,35                |



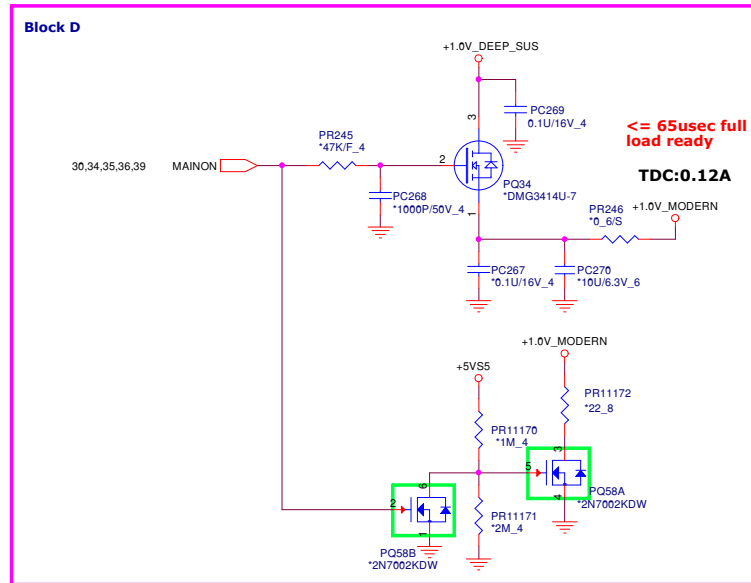
**If support Modern standby mode stuff Rb/Rc remove Ra**

**<= 65usec full  
load ready**

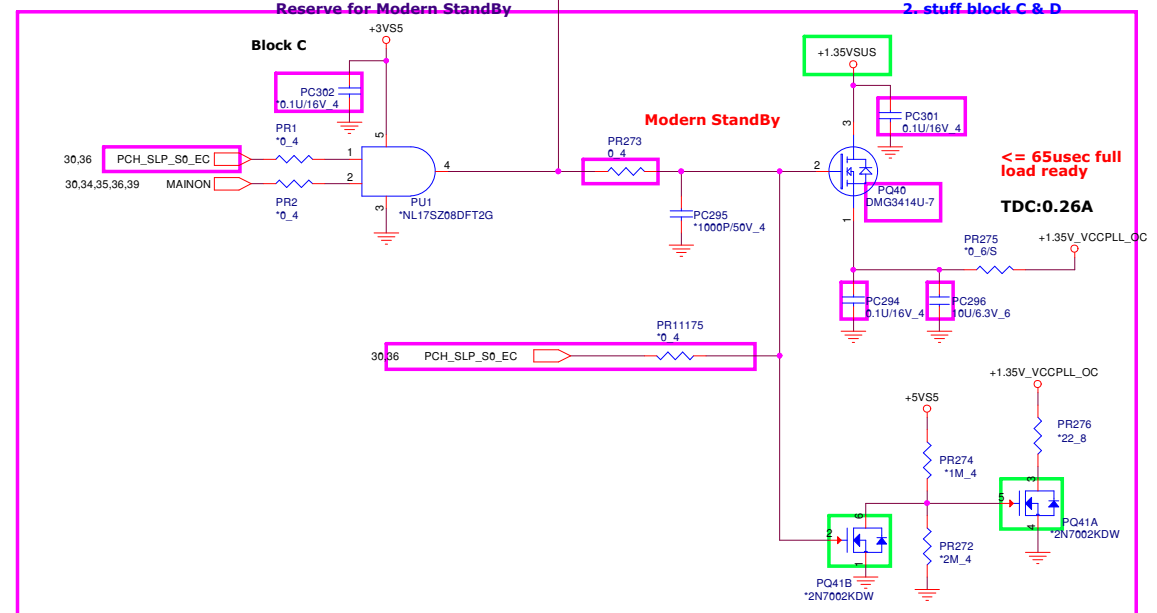


**Support Modern standby mode**

1. Remove Ra/Rc & stuff Rb/Rd
2. stuff block C & D

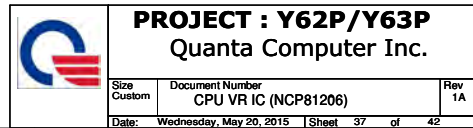


### Reserve for Modern StandBy

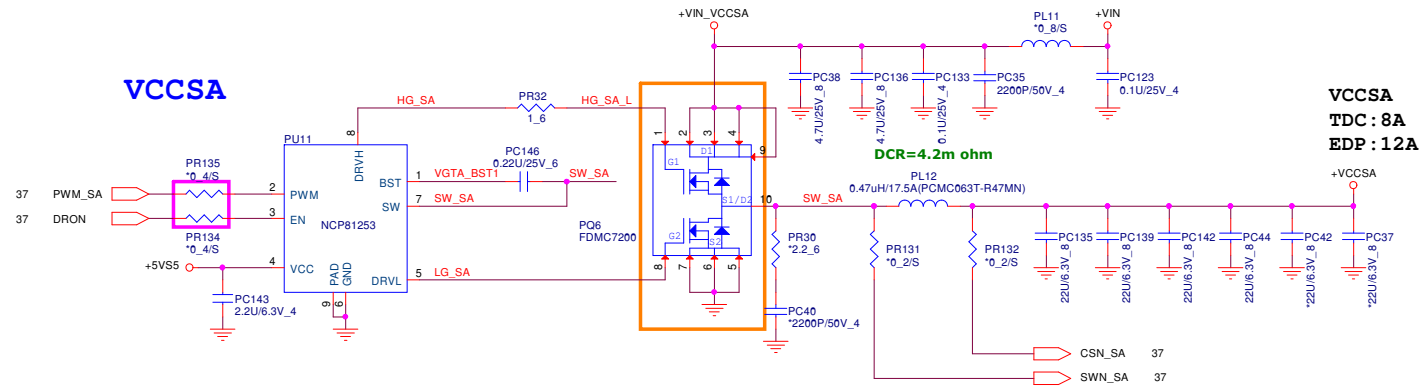


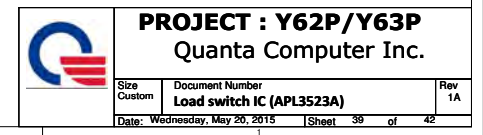
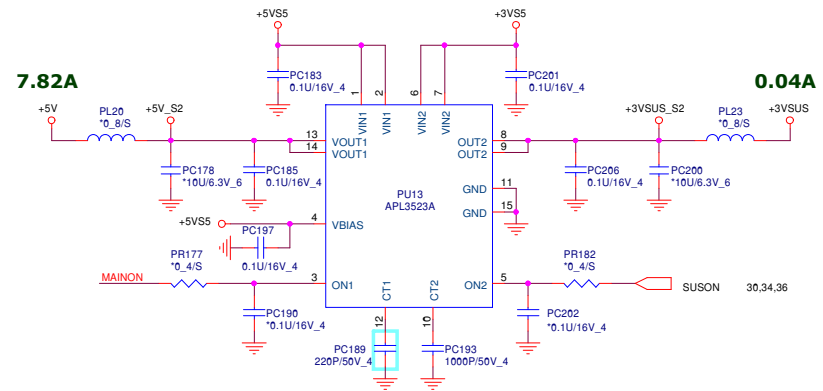
**PROJECT : Y62P/Y63P**  
Quanta Computer Inc.

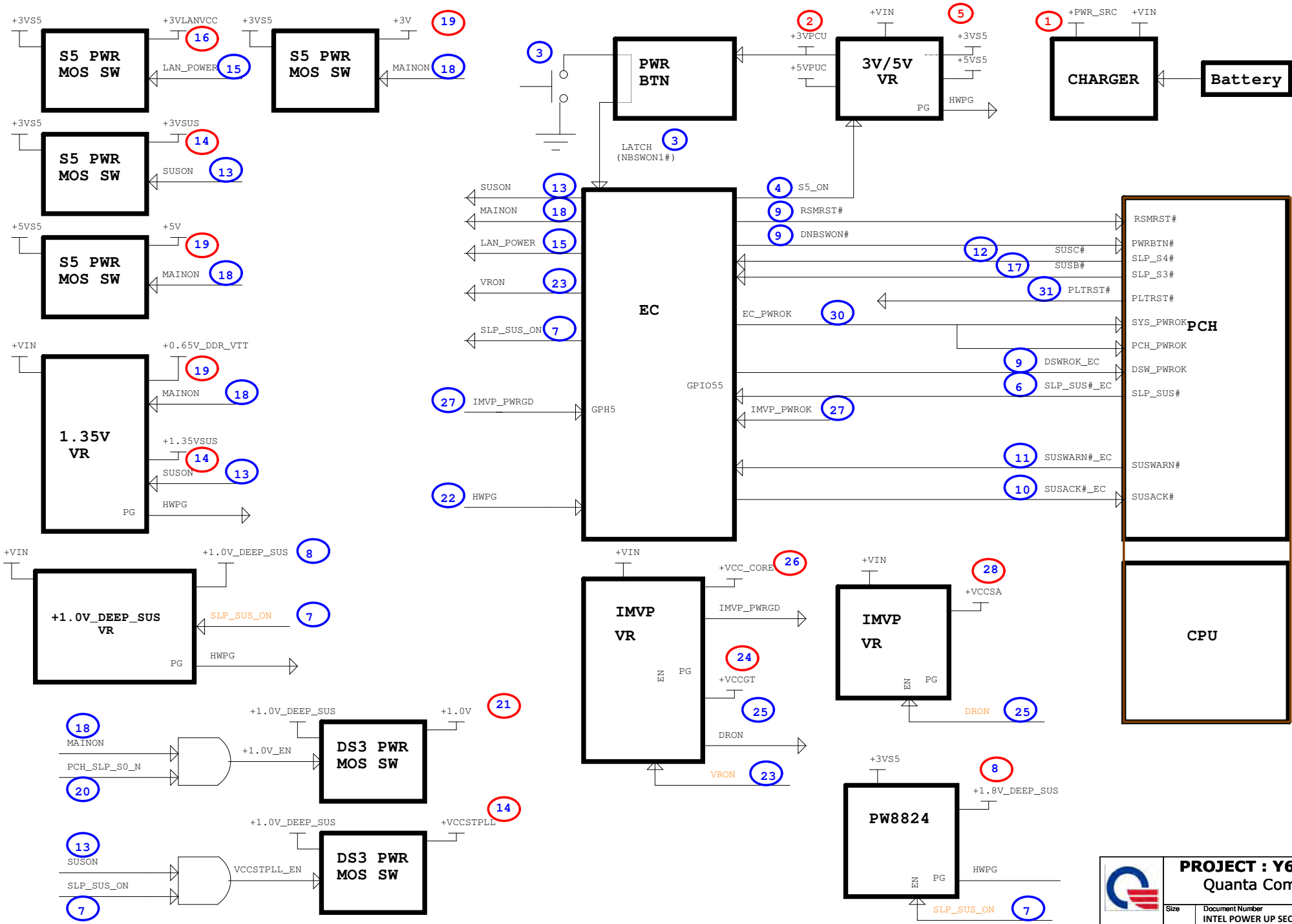
|                               |   |           |
|-------------------------------|---|-----------|
| Size<br>Custom                | Document Number<br><b>+1.0V/+VCCSTPLL</b> | Rev<br>1A |
| Date: Wednesday, May 20, 2015 | Sheet 36                                  | of 42     |



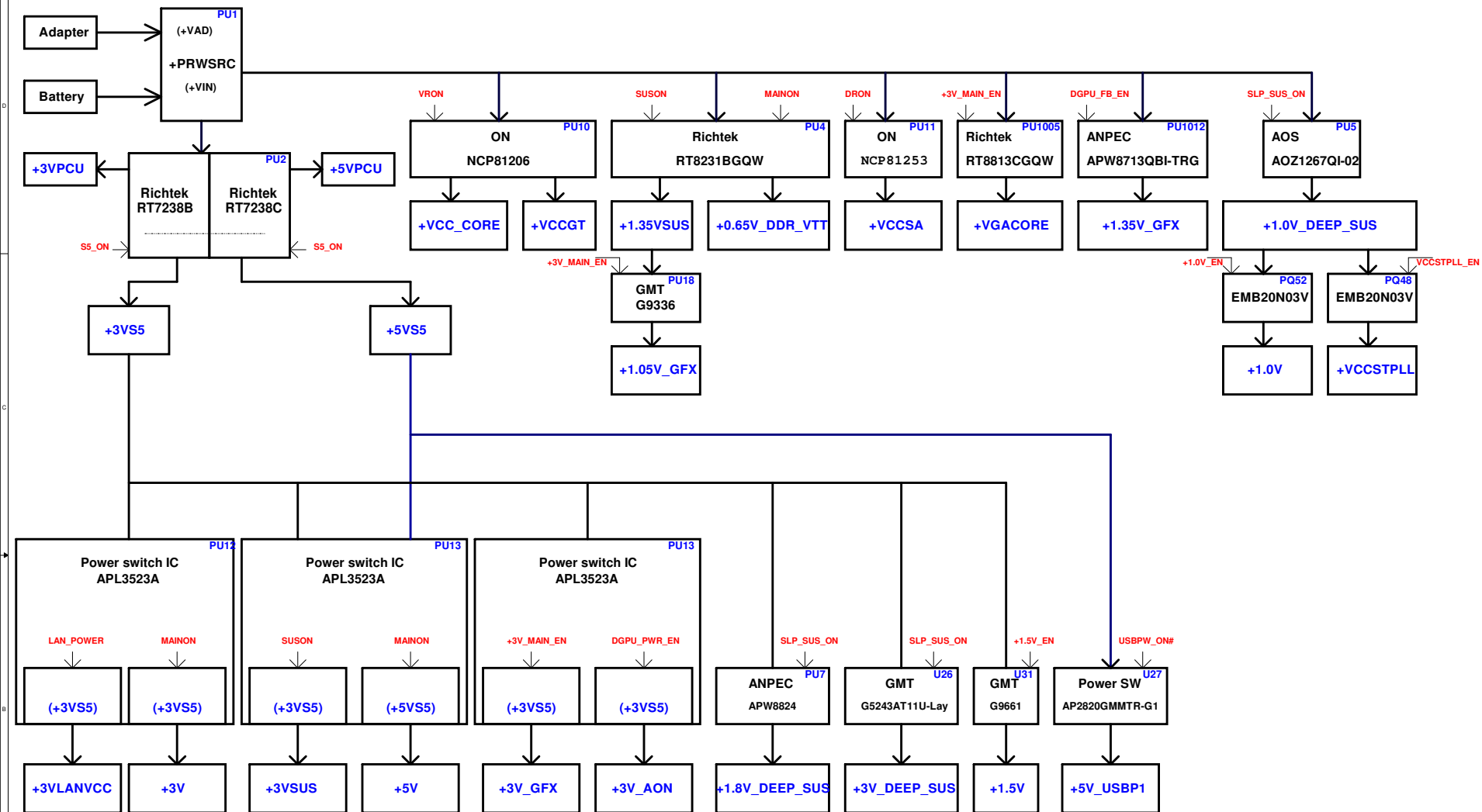
+VIN 20,27,32,33,34,35,37  
 +5VS5 4,23,25,33,34,35,36,37,39  
 +VCCSA 6,37





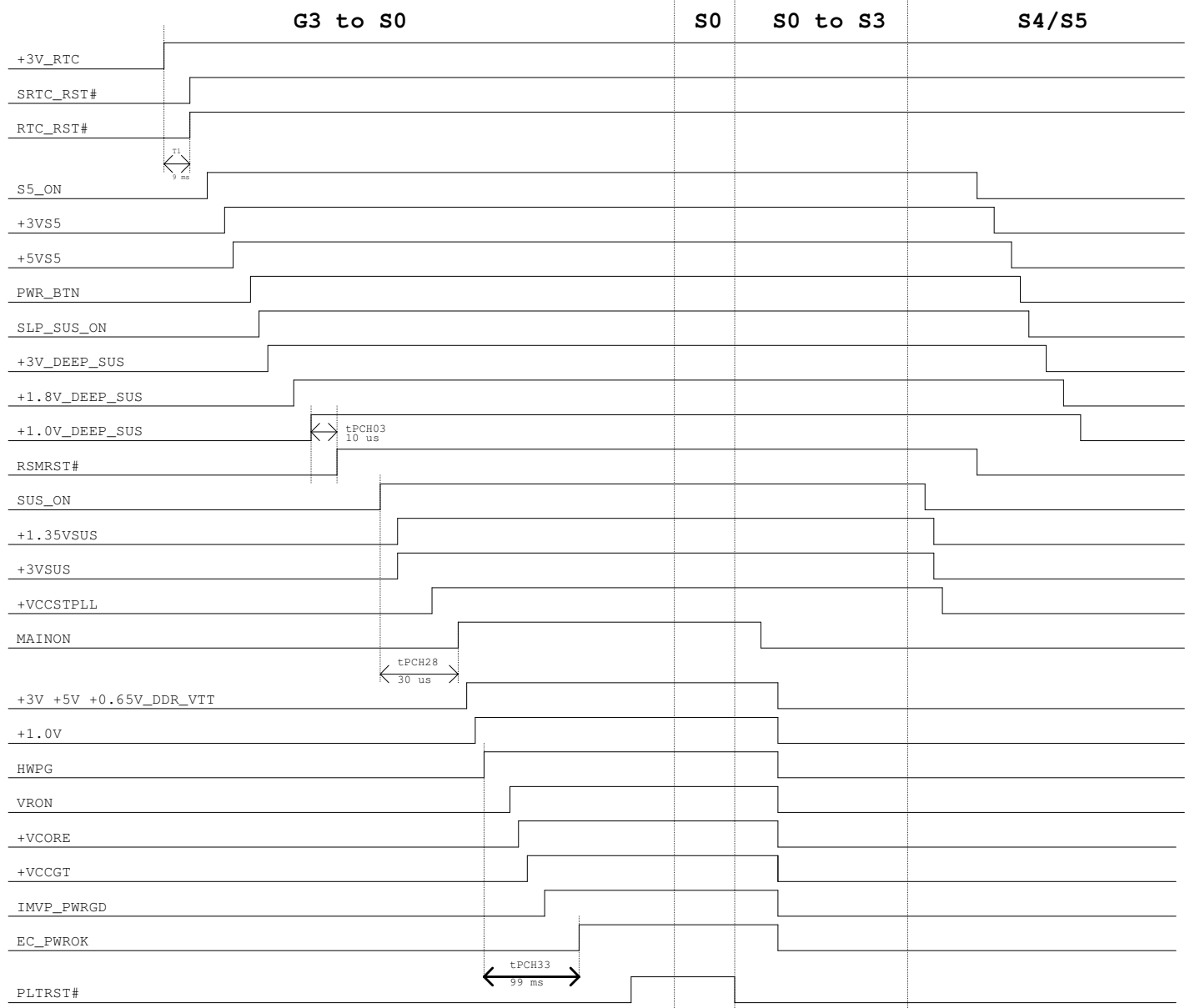






**PROJECT : Y62P/Y63P**  
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|       |                            |                |
|-------|----------------------------|----------------|
| Size  | Document Number            | Rev            |
|       | <b>Power Block Diagram</b> | 1A             |
| Date: | Wednesday, May 26, 2015    | Sheet 41 of 42 |



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|-------|-------------------------|----------------|
| Size  | Document Number         | Rev            |
|       | Intel POWER UP SEQUENCE | 1A             |
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